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# Solution processed IZTO thin film transistor on silicon nitride dielectric layer

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ABSTRACT

Solution process-based inorganic indium–zinc–tin oxide semiconductor layer was applied to fabricate a thin film transistor (TFT) by annealing at 600 °C on plasma enhanced chemical vapor deposited (PECVD) silicon nitride ($SiN_x$) dielectric layer. The spin-coated indium–zinc–tin oxide (IZTO) transistor has a field-effect mobility of 4.36 $cm^2/V\,s$ with on/off ratio of $10^5$ having the subthreshold voltage shift of 0.537 V/dec. The device characterization and surface analysis after annealing were performed and compared with results before annealing. Our results offer the feasibility of solution-based oxide semiconductor transistors for cost-effective display or other electronic devices.


## 1. Introduction

Recently, solution processed thin film transistors formed by spin coating, direct printing, and roll coating have provided a new insight over vacuum deposition process in simplicity and high performance [1,2]. Especially for a direct printing or patterning of semiconductor, such as inkjet printing, primary advantage of the solution process lies in reducing the number of processes, e.g. photolithography, required to form the semiconductor patterns [2–4]. However, most of researches about soluble semiconductor materials have been more focused on organic materials than inorganic materials due to its easy solution-processable nature. In spite of the advantage of the organic materials, the organic semiconductors could not show the desirable characteristics compared to inorganic materials, which provide high mobility, high quantum efficiency, long device lifetime, etc. [2,4,5]. For example, it was reported that silicon precursor of soluble medium could be adopted to have a high mobility TFT (thin film transistor) of around 100 $cm^2/V\,s$ [2]. Still, researches to form an inorganic semiconductor material by solution process have been less reported compared to those performed with organic materials. Very recently, many groups have emerged to fabricate semiconductor layers forming TFTs or other electronic devices based on inorganic solution [1–8]. Typically, the soluble medium includes precursors or nanoparticles of semiconductor [6]. In these cases, precursors or nanoparticles were adopted to form TFTs of mobility including amorphous oxide semiconductor (AOS) films with mobility of 16.1 $cm^2/V\,s$ or 30 $cm^2/V\,s$ [1,4–6]. For the soluble inorganic semiconductor, poly-silicon channel layers were reported to be prepared by spin coating with the mobility of around 100 $cm^2/V\,s$ [2]. However, a special silicon precursor and very stringent process controls, such as low oxygen level in a dry box, laser re-crystallization, and thermal annealing were inevitable for the process.

Promising alternatives to Si-based semiconductor, AOSs including zinc oxide (ZnO) or multi-component of zinc–indium oxide (ZIO), gallium–zinc oxide (GZO), zinc–tin oxide (ZTO), and indium–gallium–zinc oxide (IGZO) TFTs, have drawn much attentions as an active element for TFTs [3,6–8]. In order to control carrier concentration with those oxide TFTs, defect density of the ZnO or the doped-ZnO film itself should be carefully controlled [3,6]. Additionally, depending on the processing condition of doping, the environment of annealing process, and the amount of oxygen during film formation, the ZnO-based films showed both semiconducting and metallic characteristics [8]. In fact, amorphous oxide semiconductor has been studied extensively as active layer for TFTs, which were prepared by pulsed laser deposition and rf magnetron sputtering [6,7]. For example, $In_2O_3$, $Ga_2O_3$, and ZnO ternary systems under vacuum deposition have been explored as amorphous oxide semiconductors showing high mobility and on/off ratio in the range of 2–100 $cm^2/V\,s$ and $10^5$–$10^8$ [1,6]. However, those devices needed the high vacuum system to deposit films.

In this study, metal halide precursors as the soluble mediums were prepared in acetonitrile and spin coated on plasma enhanced chemical vapor deposited (PECVD) silicon nitride ($SiN_x$) to form smooth amorphous metal oxide on the dielectric layer, which is

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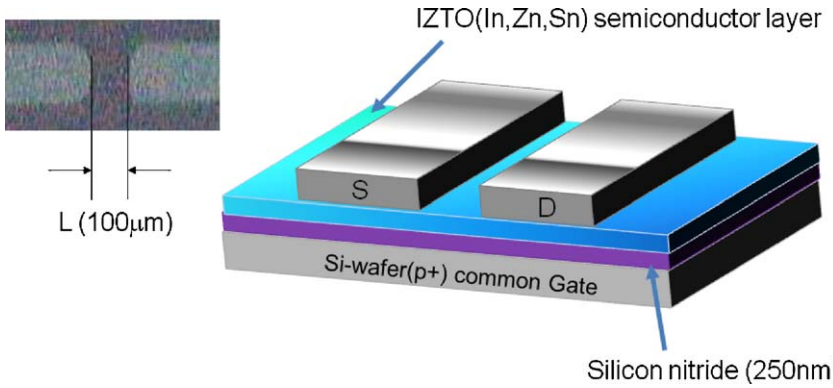


**Fig. 1.** A schematic diagram of TFT structure including a top-view microscopic image of fabricated TFT.

different from the common dielectric layer of silicon oxide like previous reports [3–5]. In addition, we fabricated amorphous indium–zinc–tin oxide (IZTO) TFTs on the $SiN_x$ layer with an additional surface treatment of sodium hydroxide, which resulted in relatively higher mobility of the oxide TFT than oxide TFTs without the treatment [9]. Device performances as well as film properties were investigated and discussed.

## 2. Experimental

For indium–zinc–tin oxide (IZTO) TFTs fabrication, a heavily boron (p+) doped silicon substrate was served as the gate in an inverted-gate structure having resistivity of 0.01–10 Ωcm. The gate insulator, 240 nm of silicon nitride ($SiN_x$), was deposited on top of the silicon substrate by plasma enhanced vapor deposition (PECVD). The IZTO channel layer was coated by spin-coater. On top of the IZTO layer, 200 nm thick aluminum layers for source/drain contacts were then evaporated. The electrodes channel width to length ratio was 2 (width 200 μm and length 100 μm). The source/drain layers were patterned through shadow masks.

IZTO solutions for fabricating spin-coating thin films were prepared by dissolving $InCl_3$ (0.02 M), $ZnCl_2$ (0.02 M) and $SnCl_2$ (0.02 M in a solvent with a volumetric ratio of 35% of acetonitrile and 65% of ethylene glycol. In order to handle the hydrophilic property of the $SiN_x$ surface, the substrate was treated with 1 M of sodium hydroxide for 8 min in an ultra-sonicator and then cleaned

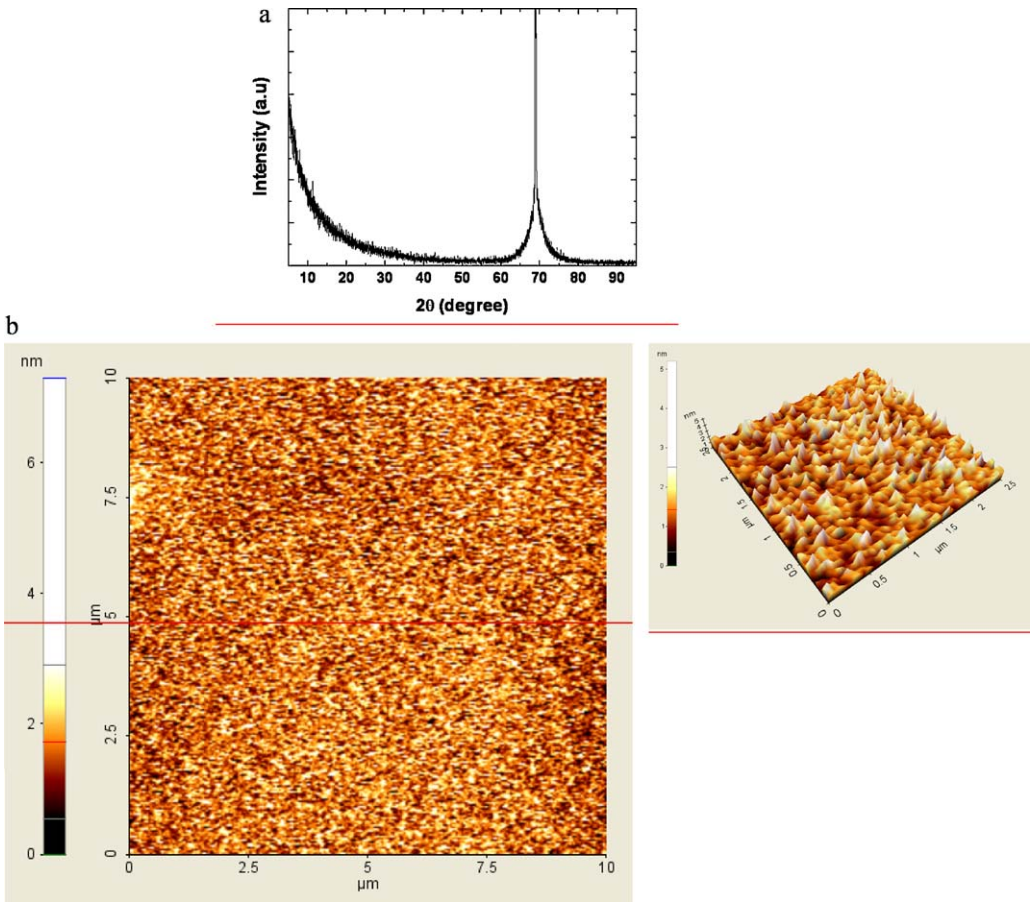


**Fig. 2.** (a) XRD spectra pattern and (b) an AFM image of 20 nm thick oxide semiconductor film on 240 nm thick silicon nitride.

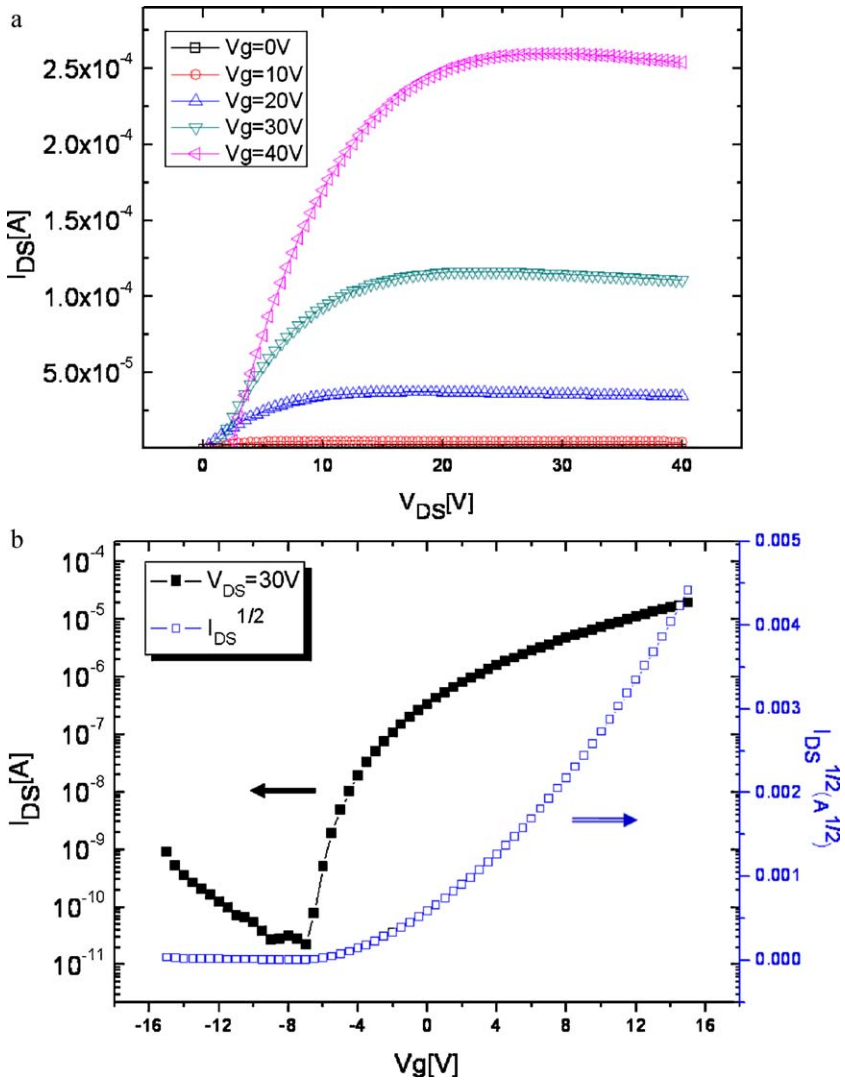


**Fig. 3.** (a) The output curve and (b) the transfer curve of the IZTO TFTs.

with DI water. The deposited thin films were dried at 100 °C for 10 min to remove solvent and annealed at 600 °C under air for 1 h in order to make oxide active layer.

Annealed IZTO surface was analyzed by AFM (Park systems XE-100, Korea). Elemental concentrations of the IZTO films were analyzed by Auger electron spectroscopy (AES: PHI660, Perkin-Elmer). Output and transfer characteristic measurements for the TFTs were performed by HP 4145B semiconductor parameter analyzer at room temperature in a dark environment.

## 3. Results and discussion

Fig. 1 shows a schematic diagram of TFT structure including a top-view microscopic image of the fabricated TFT. The device has a heavily doped P-type Si as a common gate. Indium–zinc–tin oxide (IZTO) film after 600 °C annealing was the active layer with Al source/drain electrodes to compose of the thin film transistor. Fig. 2(a) shows the XRD patterns of IZTO thin-films annealed at 600 °C for 1 h. The samples show no crystalline diffraction peaks, except for a sharp peak $2\theta \sim 68.83$ resulting from Si substrate, indicating that the spin-coating IZTO thin films are amorphous phase. Fig. 2(b) shows an AFM image of 20 nm thick oxide semiconductor film on 240 nm thick silicon nitride. The AFM image shows a clear and uniform surface morphology. There were no significant grains and grain boundary due to its amorphous nature. The surface roughness of the amorphous IZTO film was measured as 0.6 nm. In addition, there were no separate phases from the film. Fig. 2 is for 10 μm × 10 μm. It is known that there is a substitution reaction between $H_2O$ and metal halide to form the oxide semiconductor [3,4]. Therefore, an aprotic solvent, which is very volatile and does not dissociate the metal halide precursor, was adopted. Additionally, the film orientation is known as a critical factor for the performance of inorganic semiconductor. In this experiment, the amorphous-phase semiconductor will be preferred in consideration of process temperature (600 °C annealing) as reported [3–5].

Fig. 3 shows (a) the output curve and (b) the transfer curve of IZTO TFTs. Fig. 3(a) shows a conventional output characteristic of n-channel TFT with a saturation that shows a pinch-off, which indicates that there are low contents of mobile impurities inside of IZTO film [8]. Fig. 3(b) shows the transfer characteristic and the square root of the drain current versus gate voltage. The Fig. 3(b) represents the saturation mobility of 4.63 $cm^2$/V s and the threshold voltage ($V_{th}$) of 2.1 V. The on/off ratio was $10^5$ with a relatively high off current, which is expected to be much lower with patterned IZTO film. Turn on voltage ($V_{turn\text{-}on}$) in Fig. 3(b) is measured around

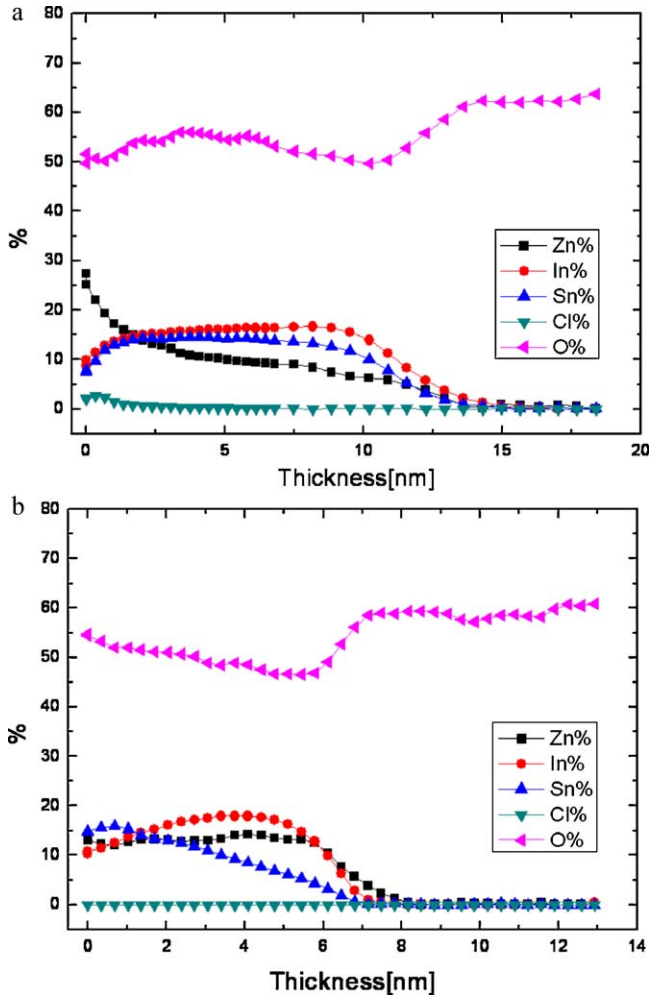


**Fig. 4.** Depth profiles of elements by AES inside of the IZTO films (a) before 600 °C annealing (solvent drying at 100 °C) and (b) after annealing at 600 °C.

−6.5 V, which is negatively shifted and relatively low compared with previous turn-on voltages with solution-based IZO-TFTs [3,8].

The subthreshold swing ($S$) of IZTO TFTs (0.537 V/dec) is particularly important for indicating low voltage, low power applications because it describes how well the switch turns on and off as the change of gate voltage [8,9]. The $S$ is given [9] by the following formula (1) using Fig. 3(b):

$$S = \frac{dV_{GS}}{d\log_{10} I_{DS}} \quad (1)$$

The negative shift of the turn on voltage is known to be due to a high carrier concentration inside of the semiconductor layer [1]. Therefore, a modulation of the carrier concentration is required in order to decrease the negative shift. In this study, it could be one of the carrier modulation methods to control the zinc/indium and tin content ratio [3], since the doped elements such as indium or gallium are known to substitute zinc sites in the lattices [4,8]. However, no clear evidence of substituting zinc/indium sites for tin was detected in this study. Fig. 4 shows depth profiles of elements inside of the IZTO films by Auger electron spectroscopy (AES), (a) before 600 °C annealing (solvent drying at 100 °C) and (b) after annealing at 600 °C. The dopants type and their concentrations can play a critical role in either suppressing or activating charge carrier generation in the oxide semiconductor system [1,4]. The IZTO film in Fig. 4(a) was not conductive to be an active semiconductor layer for the TFT. Fig. 4(a) and (b) also shows that the IZTO film was shrinked approximately 40% from 18 nm to 13 nm after annealing. In addition, before annealing, residual chlorine was detected at the top surface of IZTO film in Fig. 4(a) [3]. After the 600 °C annealing, it is clear shown that most of chlorine elements were removed by substitution reactions with water as shown in Fig. 4(b). Even without the 600 °C annealing in Fig. 4(a), the residual chlorine was less than 2% at the film depth of 2 nm. Fig. 4(b) also shows that oxygen content was the lowest at the interface with the dielectric silicon nitride. It indicates a possibility of charge carrier generation via doubly charged oxygen vacancy for high mobility [6,8]. However, more detailed studies are required. In addition, molar ratio of (zinc or indium)/tin in Fig. 4(b) was approximately measured as 2:1 at the surface. However, the concentration of the tin decreases along with the film's thickness. The reason for drastic change of tin proportion throughout the oxide film can be from the high annealing temperature of 600 °C, which is relatively close to the boiling temperature of tin chloride (623 °C). The change of the tin concentration in Fig. 4(b) also can represent for formation of the amorphous structure after the 600 °C annealing as confirmed in Fig. 2(a) [3]. Unlike the tin's concentration profile, zinc's profile was greatly changed to be evenly distributed throughout the film after annealing as compared between Fig. 4(a) and (b). The uniformly distributed zinc concentration is expected to be one of the reasons for the formation of the effective IZTO semiconductor film after the annealing.

## 4. Conclusions

Solution processed IZTO TFTs on silicon nitride gate insulator were fabricated and investigated for its performance. The IZTO film was formed in amorphous phase after high temperature annealing of 600 °C. The on/off current ratio of the IZTO TFT was $10^5$ and the field effect mobility in the saturation region was 4.36 $cm^2/V$ s with threshold voltage of 2.1 V. The results demonstrate a high possibility of using the solution-based oxide semiconductor transistor for a potential application to mass producible display.

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