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Controlling dislocation positions in silicon germanium (SiGe) buffer layers by local oxidation

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ABSTRACT

The method of controlling dislocation positions via local oxidation of 80 nm thick $Si_{0.8}Ge_{0.2}$ buffer layer on Si substrate is investigated. The strained SiGe layer is locally exposed to oxidation by patterning Si_3N_4 mask layer on SiGe with perpendicularly crossing stripe patterns with <110> directions. The local oxidation of patterned SiGe regions leads to increased stress to the remaining SiGe either via Ge pileup or volume expansion during oxidation. The increased stress in the SiGe region underneath the oxide increases dislocation nucleation rate. The preferential nucleation of dislocations and subsequent propagation of dislocations through non-oxidized regions results in reduced threading dislocation density to $10^{6-7}/cm^2$, which is lower than that of the conventional constant composition SiGe buffer layer. Further reduction of threading dislocation density is expected by optimizing the oxidation conditions and pattern size and shape for local oxidation.

1. Introduction

Epitaxially grown SiGe buffer layer on Si substrate has been investigated for various electronic and optical devices [1–3]. In particular, the strain relaxed SiGe buffer layer has been aimed to be a virtual substrate for high mobility strained Si devices because the lattice of relaxed SiGe layer is larger than that of Si, thus making it possible to grow tensile strained Si layer on SiGe buffer layer. Besides growing tensile strained Si directly on SiGe buffer layer, the SiGe buffer layer can be used as a donor substrate for the strained Silicon-on-Insulator (sSOI) [4] and strained SiGe-on-Insulator (sSGOI) [5].

Relaxed SiGe buffer layer is a practical material platform for achieving buffer layers of larger lattice than that of Si. However, there are several obstacles to overcome for the practical applications. One of them is the high density of threading dislocations which are detrimental to device properties by reducing the lifetime of minority carriers and inducing leakage current of devices. The dislocations are introduced at the interface between SiGe and Si to relax the strain of SiGe when the thickness of SiGe exceeds the critical thickness. Generally, during the relaxation process, only the misfit segments of the dislocation half-loops contribute to relaxing the in-plane strain. Consequently, the misfit segments of dislocation, as opposed to threading dislocations, are desirable to be a virtual substrate having larger lattice than Si. However, the threading arms (threading dislocations) associated with dislocation half-loops are undesirable. The goal of relaxed SiGe buffer layer fabrication methods is thus to maximize the ratio of misfit to threading dislocation density. Moreover, a flat surface is required to reduce interface scattering associated with undulation of the substrate interface.

One of the typical approaches to reduce the threading dislocation density is compositionally grading Ge in the SiGe buffer layer where Ge composition in SiGe is gradually increased [6,7]. In the case of a SiGe layer of constant composition (i.e. not graded), dislocations nucleate almost simultaneously during growth and interact and entangle with one another at the interface between the SiGe and Si substrate, thus inhibiting dislocations from propagating to long distances. Such interaction between dislocations leaves a large number of threading arms on the surface of the SiGe layer. In contrast, in the graded SiGe layer, the nucleation of dislocations across the surface is mitigated by reducing the strain accumulation rate during relaxation of SiGe layer. Consequently, the interaction between dislocations is reduced and the density of threading dislocations on the surface of the SiGe layer is reduced. The density of threading dislocations in constant SiGe layer has been reported to be around $10^{8-9}/cm^2$ while that in graded SiGe layer is around $10^{4-5}/cm^2$ [6,7]. However, the Ge grading rate should be low, typically at or less than

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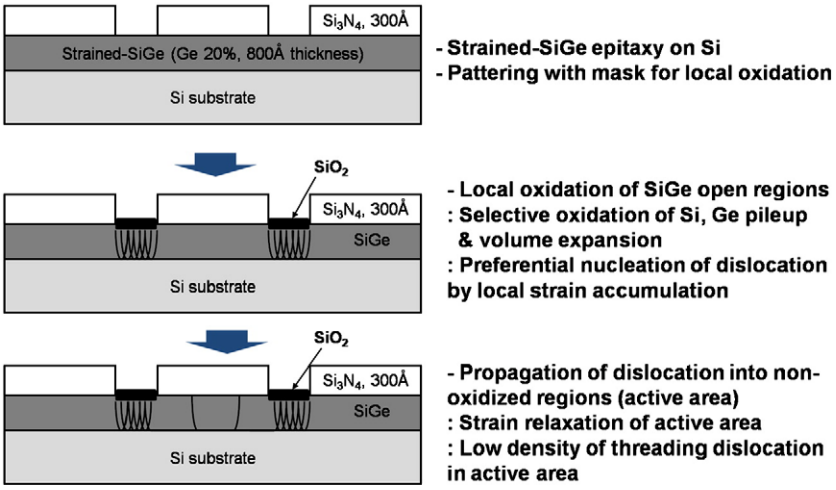

Fig. 1. Schematic illustration of local oxidation process for controlling dislocation positions in the SiGe buffer layer.

10%/μm in order to obtain reduced threading dislocation density. This consequently requires a large thickness of graded SiGe buffer layer, which is a drawback because of the increased production costs and increased thermal resistance. In addition, the strain-relaxed graded SiGe buffer layer generally has a rough surface [8,9].

Another approach to reduce the threading dislocation density has been reported by employing a low temperature Si buffer layer prior to growing a SiGe layer [10]. In addition, ion implantation after growing a strained SiGe layer and subsequent annealing has been reported as a potential solution to reduce threading dislocation density [11]. Generally, these methods function by introducing non-equilibrium point defects in the layers and then inducing the clustering of point defects to relax the strain. This results in a low density of threading dislocations less than $10^4/cm^2$. However, the density of threading dislocation is still much higher than a typical surface pit density on the order of $0.01/cm^2$ on Si substrate [12]. Moreover, threading dislocations are randomly distributed across the entire substrate. This random distribution of threading dislocations may result in deviation of the properties of individual devices formed on the substrate.

It would be best that a relaxed SiGe buffer layer has no threading dislocations on the entire surface of SiGe layer. However, from a device fabrication point of view, it is not necessary for the entire surface to be free of threading dislocations. In current semiconductor device designs, individual devices are fabricated on active area and are separated by trench isolation regions with SiO_2. Thus, it is sufficiently acceptable that only the active area of the surface where devices are to be fabricated is free of threading dislocations by controlling the dislocation distribution.

Attempts have been made to control the location of dislocation by forming patterned Si mesa structures. For example, Fitzgerald et al. reported a process of fabricating a patterned Si mesa structure and then growing a SiGe layer thereon [13]. The patterned mesa structure reduces the threading dislocation density by limiting the dislocation interaction at small growth areas and then allowing the threading segments to escape at the mesa edge. Also, Watson et al. attempted to control dislocation nucleation during SiGe layer growth on Ge implanted Si regions that were previously patterned before implantation [14]. However, the use of mesa structures raises complications because the non-planar mesa structure is fundamentally incompatible with planar Si VLSI technology.

In this study, the method for controlling dislocation position in SiGe buffer layer grown on Si substrate is discussed by employing local oxidation of SiGe. The local oxidation of SiGe layer is aimed to produce high quality relaxed SiGe buffer layer as a virtual substrate with flat surface and low density of threading dislocations for strained Si device applications. In order to achieve the threading dislocation free active area, in this approach, the dislocation half-loops are intentionally induced to nucleate only at the patterned regions of which surface are oxidized and ultimately used as isolation regions, by local oxidation process.

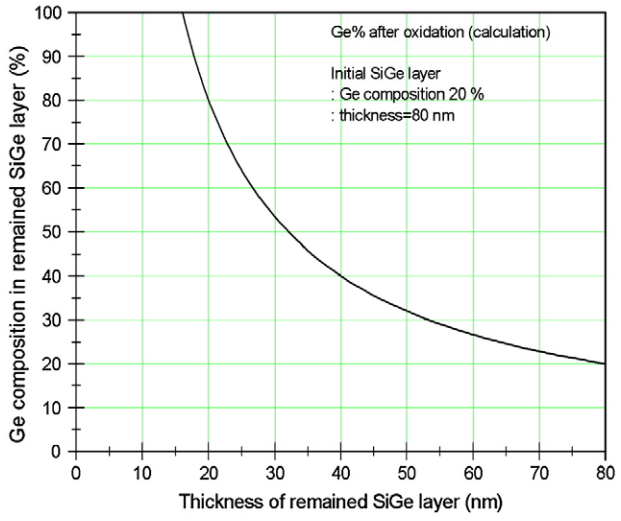

Fig. 2. Calculation of Ge composition as a function of the thickness of the remaining SiGe layer after oxidation.

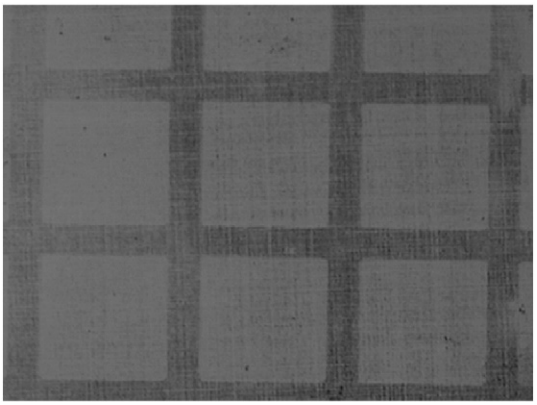

Fig. 3. Optical microscopy images of SiGe surface after removing Si_3N_4 mask and SiO_2 layer and Secco etching. The square pattern of the non-oxidized region has a size of $200 \times 200\ \mu m^2$.

2. Experimental

In order to carry out the local oxidation process, the epitaxial $Si_{0.8}Ge_{0.2}$ layers with a constant composition of Ge 20% were grown using a Riber EVA-32 molecular-beam epitaxy (MBE) system. The Si substrates were cleaned with a modified Piranha method before being loaded into the growth chamber by immersing the substrates in Piranha solution (H_2O_2:H_2SO_4 = 3:5) for 1 min and then in aqueous HF solution (HF:H_2O = 1:10) for 1 min. This procedure was repeated three times. Subsequently, the substrate was in-situ cleaned in the growth chamber by desorbing the native oxide at 800 °C for 10 min with Si flux. After all the cleaning procedures, a SiGe layer was grown at 550 °C with a growth rate of 0.95 Å/s. The thickness of the SiGe layer was 80 nm that is below the critical thickness for dislocation introduction at the growth temperature of 550 °C [15].

For the local oxidation of SiGe open regions, the oxidation mask layer with 30 nm thick Si_3N_4 was deposited and patterned as stripe lines with perpendicularly crossing <110>directions through optical lithography and reactive ion etching of Si_3N_4 layer. The width of the stripe pattern is about 50 μm and the non-oxidized regions have a size of 100×100 and 200×200 μm^2. The open regions of SiGe were selectively oxidized by dry oxidation at 800 °C for 1 h, during which the 10 nm thick SiO_2 layer was formed on the SiGe layer. A Si_3N_4 mask layer was subsequently removed by wet etching with 85% H_3PO_4 solution at 160 °C. The surface of the SiGe layer and threading dislocation density were analyzed by optical microscopy and scanning electron microscopy (SEM) after removing SiO_2 by wet etching with HF solution and defect etching of SiGe surface with Secco etchant [16]. In addition the dislocation distribution was characterized by plan-view and cross-sectional transmission electron microscopy (TEM).

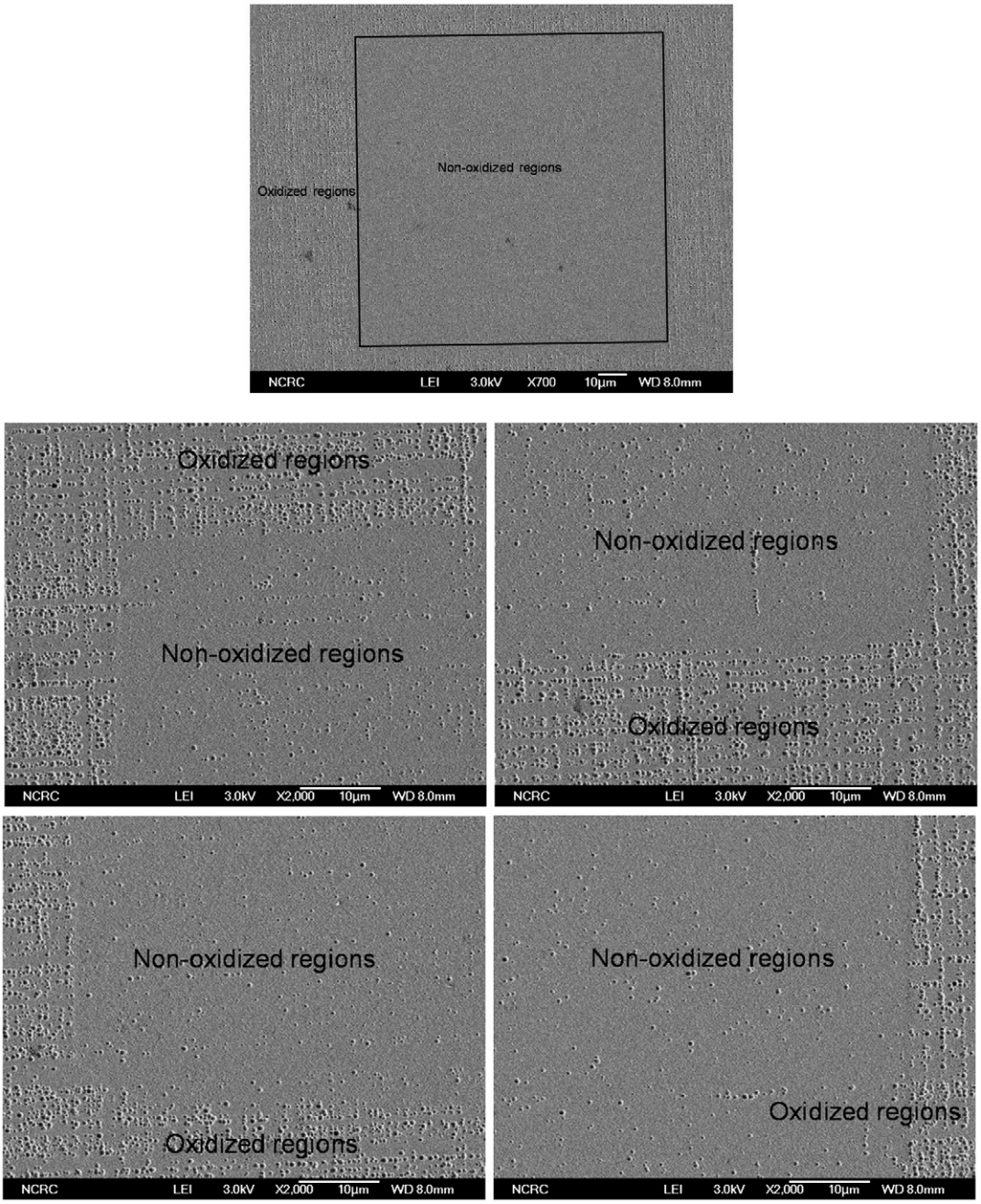

Fig. 4. SEM images of SiGe surface after removing Si_3N_4 mask and SiO_2 layer and Secco etching. The square pattern of the non-oxidized region has a size of 100×100 μm^2.

3. Results and discussion

Fig. 1 is the schematic illustration of local oxidation process for controlling dislocation positions in SiGe buffer layer. First, an epitaxial, strained SiGe layer was grown on Si substrate. The thickness of SiGe layer is below the critical thickness for dislocation introduction. Otherwise, the dislocations would have been introduced during growth and lots of threading arms be left on entire surface. After growing the SiGe layer, the oxidation mask layer such as Si_3N_4 layer is grown and patterned as stripe lines with perpendicularly crossing <110>directions. Thus, the SiGe regions with stripe patterns having <110> directions are exposed. Subsequently, the exposed regions of SiGe are selectively oxidized by dry oxidation during which SiO_2 is formed on the SiGe layer. The oxidation is expected to result in the preferential formation of dislocations at the oxidized region by the following reasons. One of them is that the increased strain at SiGe underneath the oxide due to Ge pileup by the selective oxidation of Si during SiGe oxidation increases dislocation nucleation rate. The higher strain in the SiGe layer underneath the oxide than that in non-oxidized regions leads to the higher nucleation rate of dislocations at the oxidized regions. The volume expansion of top oxide during oxidation also adds the compressive strain to underlying SiGe and promotes the dislocation nucleation. In addition, the interstitials of Si and Ge atoms into underlying SiGe layer that are generated during oxidation facilitate the dislocation nucleation. All of these effects support the preferential nucleation of dislocation at the oxidized regions.

During the oxidation or subsequent annealing step, the dislocations at the oxidized regions propagate from one oxidized regions to another by permitting the misfit segments to relax the strain of non-oxidized SiGe. The net result is that the oxidized regions may act as sources as well as barriers/sinks for the dislocation half-loops.

In this approach, while the entire surface of the substrate has an average threading density greater than the conventional relaxed buffer layers, the density is concentrated in the oxidized regions where the devices are not built. The oxidized regions may be used for isolation regions, thereby reducing any possibility to waste areas of the substrate. Another advantage of this approach comes from using an oxidation mask layer which acts as a dislocation nucleation-inhibiting layer at non-oxidized regions. The oxidation mask layer prevents nucleation of dislocation loops at a free surface of the SiGe layer.

Fig. 2 shows the calculation of Ge composition as a function of the thickness of remaining SiGe layer after oxidation assuming the complete pileup and uniform redistribution of Ge atoms in SiGe layer underneath SiO_2. During the oxidation, Si and Ge can be oxidized as forming SiO_2 and GeO_2, respectively. Subsequently GeO_2 reacts with neighboring Si atoms and forms SiO_2, therefore Ge atoms are piled up into the underlying SiGe layer [17,18]. As shown in Fig. 2, the Ge composition in the underlying SiGe increases as the SiGe thickness is reduced by the oxidation. In this experiment, the thickness of SiO_2 is about 10 nm, corresponding to a Ge pileup of 1–2% assuming the uniform redistribution of Ge in SiGe layer. In actual case, however, Ge is expected to be more concentrated near the interface between SiO_2 and SiGe, so the strain is more accumulated at the interface with SiO_2. It facilitates the nucleation of dislocation loops below the oxide because the dislocation nucleation rate is proportional to $\tau_{\mathrm{eff}}^{2.5}$, where τ_{eff} is the effective stress depending on misfit strain between SiGe and Si, i.e. the Ge composition of SiGe layer [15]. Actually, the strain relaxation should occur through the dislocation introduction both at the oxidized and non-oxidized regions because the thickness of SiGe layer exceeds the critical thickness for dislocation introduction during the oxidation at 800 °C. Under this condition, the preferential formation of dislocation loop at the oxidized regions can be obtained

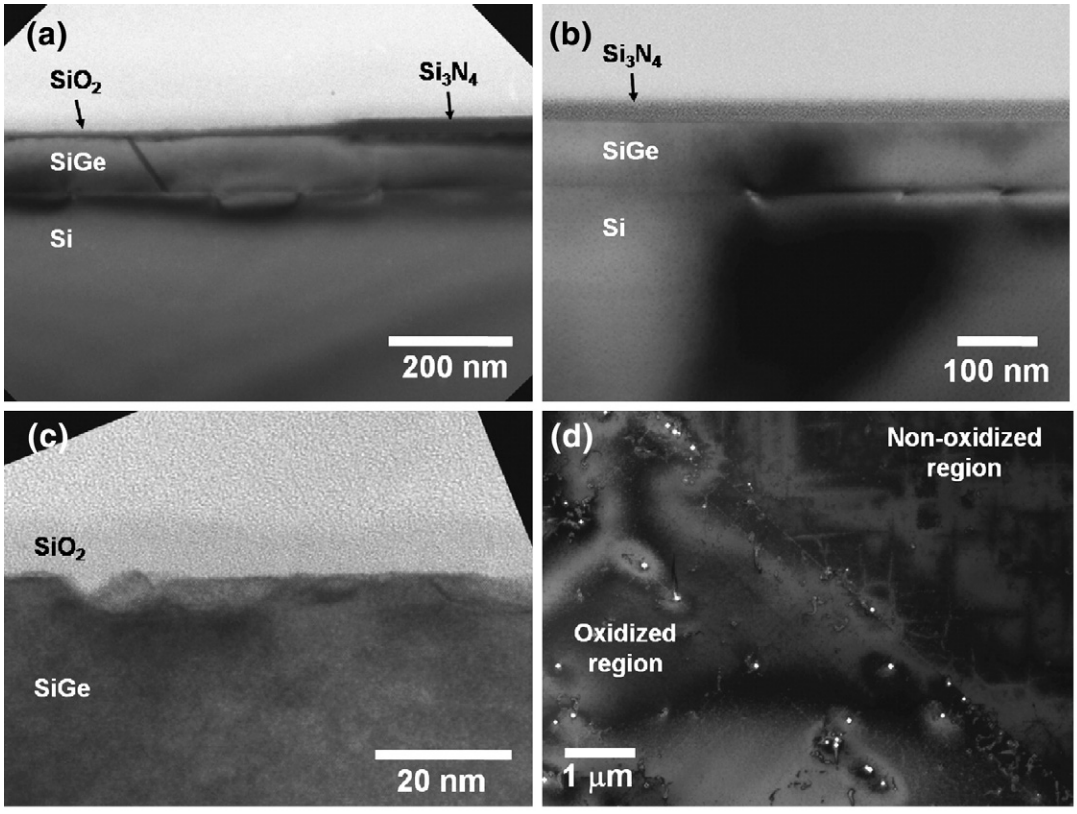

Fig. 5. Cross-sectional TEM images (a) showing both oxidized and non-oxidized SiGe layers, (b) magnified image of non-oxidized region and (c) oxidized region, and (d) plan-view image of both oxidized and non-oxidized SiGe surfaces after removing Si_3N_4 mask and SiO_2 layer.

only through the different nucleation rate between oxidized and non-oxidized regions determined by the effective stress. However, because the Ge pileup is not significant in this oxidation condition, a severer oxidation at either higher temperature or longer time should be carried out to make clearer the effect of Ge pileup for preferential dislocation nucleation.

The preferential nucleation of dislocations at the oxidized regions is clearly observed in the optical microscopy images (Fig. 3) and scanning electron microscopy images (Fig. 4) after removing the Si_3N_4 mask and SiO_2 layer and Secco etching to reveal the threading dislocations as a form of etch-pits. The SiGe at oxidized regions have much higher density of etch-pits than the non-oxidized regions. It is thought that the dislocation half-loops nucleate in oxidized regions and propagate through non-oxidized regions to relax the strain. The etch-pits are observed following <110>direction of SiGe and the density of etch-pits are abruptly reduced at the non-oxidized regions. It demonstrates the preferential nucleation of dislocations by the local oxidation process. The density of etch-pits (threading dislocations) was counted at the regions of $10\times10\,\mu m^2$ squares. The etch-pit density is about 0.6, 1.4, and $2\times10^7/cm^2$ for three patterns of non-oxidized region with a size of $100\times100\,\mu m^2$, while the density on oxidized regions is about $10^{8-9}/cm^2$. Even though there is a deviation between patterns, it can be concluded that the threading dislocation density is in the order of $10^{6-7}/cm^2$, which is lower than conventional constant SiGe buffer, but is still higher than compositionally graded one. Therefore, the oxidation and annealing conditions as well as the pattern size and shape should be optimized to further reduce the threading dislocation density.

Fig. 5(a)–(c) are the cross-sectional TEM images of oxidized and non-oxidized regions. In Fig. 5(a), the left region is the oxidized region having ~10 nm thick SiO_2 layer on SiGe and the right one is the non-oxidized region with 30 nm thick Si_3N_4 masks, which are magnified in Fig. 5(b) and (c), respectively. The misfit dislocations are found at the interface between SiGe and Si substrate at both regions. A stacking fault is also shown at the oxidized region. The threading dislocations are not found at both regions probably because the TEM samples are too thin. It is notable that the oxidized regions have rough interface between oxide and SiGe as shown in Fig. 5(c). One probable reason for rough interface is the reactive ion etching damage during the pattern formation. During the reactive ion etching of Si_3N_4 layer to open SiGe regions, the SiGe surface would be exposed and etched. The etch rate of Si and Ge atoms might be different in the Si_3N_4 etching environment. Therefore the rough surface could be formed during the patterning step by different etch rate of Si and Ge. In addition, the rough surface of SiGe can be created by the cross-hatch morphology of strain-relaxed SiGe. The wavelength of roughness of cross-hatch surface, however, is typically 1–2 μm, so the rough interface in Fig. 5 (c) having 10–20 nm wavelengths is not the cross-hatch morphology. It should be further clarified whether this rough interface is related to the Ge pileup or strain relaxation behavior.

Fig. 5(d) is the plan-view TEM image of SiGe surface after removing SiO_2 and Si_3N_4 layer. The left bottom region is the oxidized region and right top region is the non-oxidized one, which are divided in diagonal direction. In the oxidized region, the threading dislocations shown as worm-shaped defects are well observed while not at non-oxidized region, as same with SEM images in Fig. 4. It demonstrates the preferential formation of dislocation half-loops at the oxidized regions by local oxidation process.

4. Conclusion

The control of dislocation position in SiGe buffer layer by local oxidation of SiGe is demonstrated. The local oxidation of stripe pattern of SiGe layer leads to the preferential nucleation of dislocations at the oxidized regions. SEM and TEM analyses reveal that the oxidized SiGe regions have more threading dislocations than the non-oxidized regions. The resulting threading dislocation density is in the order of $10^{6-7}/cm^2$, which is lower than that of conventional constant composition SiGe buffer layer. In order to further reduce the threading dislocation density, the oxidation conditions and pattern size and shape for local oxidation should be optimized.

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