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Vertically and Laterally Self-Aligned Double Layer of Nanocrystals in Nanopatterned Dielectric Layer for Nanocrystal Floating Gate Memory Device

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The formation of a vertically and laterally self-aligned double layer of CdSe colloidal nanocrystals (NCs) in a nanopatterned dielectric layer on Si substrate was demonstrated by a repeating dip-coating process for NC deposition and atomic layer deposition (ALD) of Al_2O_3 layer. A nanopatterned SiO_2/Si substrate was formed by patterning with a self-assembled diblock copolymer. After the selective deposition of the first NC layer inside the SiO_2 nanopattern by dip-coating, an Al_2O_3 interdielectric layer and the second NC layer in the Al_2O_3 nanopattern were sequentially deposited. The capacitance–voltage measurement of an Al-gate/ALD-Al_2O_3(25 nm)/second-CdSe-NCs/ALD-Al_2O_3(2 nm)/first-CdSe-NCs/nanopatterned-SiO_2(15 nm)/p-Si substrate structure showed the flatband voltage shift through the charge transport between the gate and NCs.
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Nonvolatile nanocrystal (NC) floating gate memory device has been of considerable interest because it offers the advantage of improved scalability by using discrete charge storage nodes with NCs embedded in a gate dielectric layer. The physically and electrically isolated NCs do not allow the lateral charge loss; therefore, they store the charges more reliably even at highly scaled device structures. Moreover, the structures of double or multilayer NCs have been employed to increase the memory window by increasing the density of NCs and to further improve the retention characteristics.[1-7] In general, the repeated deposition of NCs and interdielectric layer by physical[1-4] and chemical vapor depositions[5,6] has been studied to fabricate double or multilayer NCs embedded in a gate dielectric layer. However, it produces the vertically and laterally random distribution of NCs. Because the threshold voltage shift of memory devices is determined by the stored charge density corresponding to the density of NCs, the random distribution of NCs causes the problem of distributional threshold voltage shift of devices. Thus, it limits the practical application of NC memory for highly integrated devices that operate in the same operating voltage range. Therefore, it is truly required to realize the uniform size and distribution of NCs.

Ohba et al. reported the self-aligned double layers of Si NCs by oxidizing the multilayer structure of Si NC/SiO_2/amorphous-Si/SiO_2 on Si substrate.[7] During oxidation, the lower level amorphous-Si layer was oxidized as masked by the upper Si NCs and was left as NCs below the upper NCs; therefore, the vertically aligned double layer of NC structure was fabricated. However, because the upper Si NCs were randomly deposited, their lateral arrangement was fairly random. The uniform array of NCs with identical size and density could be achieved by nanopatterning and selective formation of NCs in nanopatterns.[8-10] Black et al.[8] used poly(styrene-*b*-methyl methacrylate) (PS-*b*-PMMA) diblock copolymer as an etching mask of the SiO_2 tunneling layer and subsequently formed Si NCs by chemical vapor deposition and etchback process, which left the Si NCs only inside the patterns as being isolated each other. Also, Shahrjerdi et al.[9] used the same PS-*b*-PMMA diblock copolymer to pattern a structure of SiO_2/polyimide/SiO_2 multilayers. After etching the polyimide with a diblock copolymer and SiO_2 etching mask, Ni was deposited on polyimide nanopatterns as being isolated NCs. Then, the polyimide layer was removed by the lift-off process. They could successfully form the laterally ordered NC single layer. We also reported the laterally aligned NC formation in SiO_2 nanopatterns by a simple dip-coating process.[10] The colloidal CdSe NCs were selectively delivered into the SiO_2 nanopatterns having a diameter of ~20 nm and center-to-center distance of ~40 nm formed by the self-assembled PS-*b*-PMMA diblock copolymer by a dip-coating process. In this approach, the nanopatterned substrates were dipped into the NC colloidal solution and withdrawn with a controlled speed, during which NCs were selectively delivered inside the nanopatterns. In contrast to the previous reports using thin-film deposition in nanopatterns and etchback[8] and lift-off[9] processes, the process of selective deposition of colloidal NCs in nanopatterns by dip-coating could be utilized for the multilayer NC formation. We reported the formation of maghemite NC multilayer inside the pores of anodic aluminum oxide nanotemplates by a repeated dip-coating process.[11] This demonstrates the possible formation of vertically and laterally self-aligned NCs in nanopatterns for the NC floating gate memory.

In this study, we employed the repeated dip-coating process for selectively depositing colloidal NCs into nanopatterns with interdielectric layer deposition to realize the memory device with both vertically and laterally self-aligned double layer of NCs. To our best knowledge, the successful formation of both vertically and laterally aligned NC multilayer for NC memory has not been reported yet. The formation of vertically and laterally aligned double layer of NCs is expected to provide a better uniformity of device performances that is crucial for highly integrated devices, as well as the increased memory window and retention characteristics.

Thin films of the PS-*b*-PMMA diblock copolymer were used for the patterning of the SiO_2 layer with a thickness of 25 nm on p-Si substrate. Before coating PS-*b*-PMMA, a polymer brush layer with a thickness of 5 nm was coated to induce the balanced interfacial interaction (so-called neutrality of random copolymer brush) on the substrates, leading to the cylindrical microdomains oriented normal to the surface with a hexagonal pattern. Then, a 30 nm thick PS-*b*-PMMA layer was spin-coated and annealed at 170°C for 24 h to form the hexagonally self-assembled cylindrical patterns.[12] The copolymer pattern was transferred to the underlying SiO_2 layer by selectively removing the PMMA block and reactive ion etching of the SiO_2 layer. The etched cylindrical nanopatterns have a diameter

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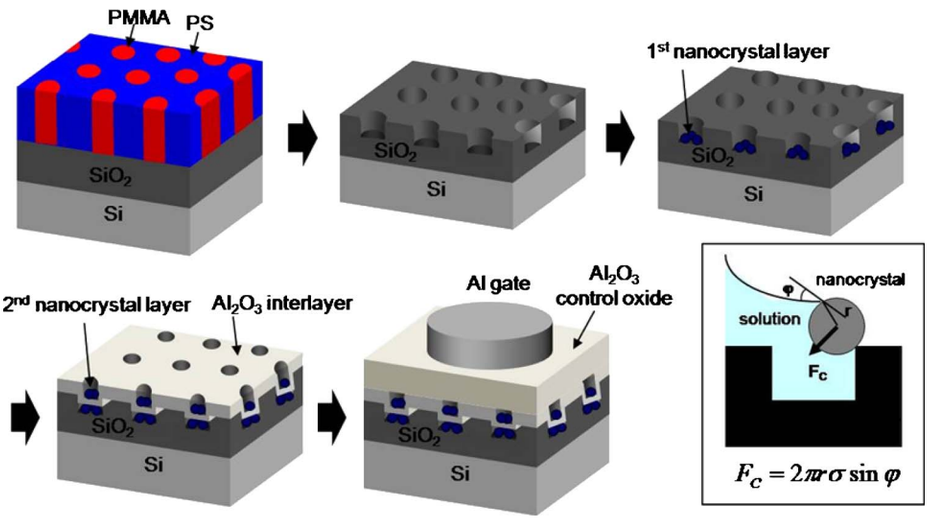

Figure 1. (Color online) Schematic illustration of the procedure of NC double-layer formation in nanopatterns and the capacitor structure for *C-V* analysis.

of ~20 nm and a center-to-center distance of ~40 nm corresponding to the pattern density of 7×10^{10} cm^{-2}. The thickness of the patterned SiO_2 after etching is ~15 nm. These substrates were dipped into the CdSe colloidal NC solution and withdrawn with a speed of 0.01 mm/s, and were dried in air at room temperature. The CdSe NCs with a diameter of ~5 nm, coated with a thin ZnS layer and trioctylphosphine oxide (TOPO) as a surfactant, were used as purchased from Nanosquare, Inc. The NCs were dispersed in octane with a concentration of an order of 10^{16}/mL. The selective deposition of NCs inside the nanopatterns was analyzed using a scanning electron microscope (SEM, Hitachi S-4800) and a high resolution transmission electron microscope (TEM, Technai F20).

The capacitor structure of the Al-gate/ALD-Al_2O_3 (25 nm)/second-CdSe-NCs/ALD-Al_2O_3(2 nm)/first-CdSe-NCs/ nanopatterned-SiO_2(15 nm)/p-Si substrate was fabricated to characterize electrical performance. After depositing the first layer of CdSe NCs into the SiO_2 nanopatterns, annealing at 200°C for 1 h was carried out to desorb the surfactants from the NC surface.[11] Then, a ~2 nm thick Al_2O_3 interlayer was deposited by atomic layer deposition (ALD) using a sequential supply of trimethylaluminum and water vapor at 200°C. The ALD is known to enable atomic-scale control of the film thickness with excellent step coverage by self-limited surface reaction. Thus, it could be successfully used for conformally depositing an interdielectric layer to form the Al_2O_3 nanopatterns on the underlying SiO_2 nanopatterns. Subsequently, the dip-coating and annealing steps were repeated to form the second layer of CdSe NCs in the Al_2O_3 nanopatterns. Then, a 25 nm thick Al_2O_3 layer was also deposited by ALD as a control oxide. Then, annealing was carried out at 700°C for 1 h in O_2 environment to improve the dielectric quality of the Al_2O_3 layer. Top Al gate was deposited with a thickness of 500 nm and a diameter of 500 μm by evaporation with a hard mask. The post-metal annealing was carried out at 450°C for 30 min in Ar environment. The procedure for NC double layer formation in nanopatterns and the capacitor structure are schematically illustrated in Fig. 1. The charging behavior was analyzed using high frequency capacitance–voltage (*C-V*) characteristics with a frequency of 100 kHz using an Agilent 4284A precision LCR meter. Both gate voltage sweeping and gate pulse programming were conducted.

Figure 2 is the plan-view SEM micrograph of the second CdSe NC layer in Al_2O_3 nanopatterns. The second layer of NCs is selectively deposited into the nanopatterns of an ~2 nm thick Al_2O_3 interdielectric layer on the first layer of NCs. As previously reported, the colloidal NCs can be selectively deposited inside the patterns by the capillary force-driven migration into the patterns.[13,14] During the solvent evaporation while withdrawing the substrate from the solution, the capillary force operates at NCs at the edge of the solution interface with the patterned surface, as schematically shown in Fig. 1. The capillary force F_c is expressed as $F_c = 2\pi r\sigma \sin \varphi$, where σ is the surface tension of a solution (roughly assumed to be 21.62 mN/m of octane solvent), *r* is the nanocrystal–solution contact line radius that is equal to the nanocrystal radius when the solution meniscus moves down to a thickness of nanocrystal radius, and φ is the angle between the radial axis of the nanocrystal and solution (assumed to be 90° of complete wetting between nonpolar octane solvent and hydrophobic tail of oleic acid covering the NC surface).[15] The force with a direction into the patterns is calculated to be ~80 kT/nm for CdSe NC with 5 nm diameter, which is strong enough to drive NCs into the patterns.[10] During dip-coating, CdSe NCs can adsorb on the top surface of SiO_2 for the first NC layer deposition and on the Al_2O_3 surface for the second layer deposition by van der Waals interaction.[16,17] The van der Waals interaction energy between the CdSe NC with a 5 nm diameter and SiO_2 substrate across the medium of octane solvent, with a distance of 1.2 nm by TOPO surfactant, is calculated to be ~0.28 kT. Also, the van der Waals energy on Al_2O_3 is ~1.15 kT. In this calculation, the Hamaker constants of CdSe, SiO_2, Al_2O_3, and octane are 0.388,[18] 0.41,[16] 0.95,[19] and 0.28 eV,[16] respectively, and the length of the

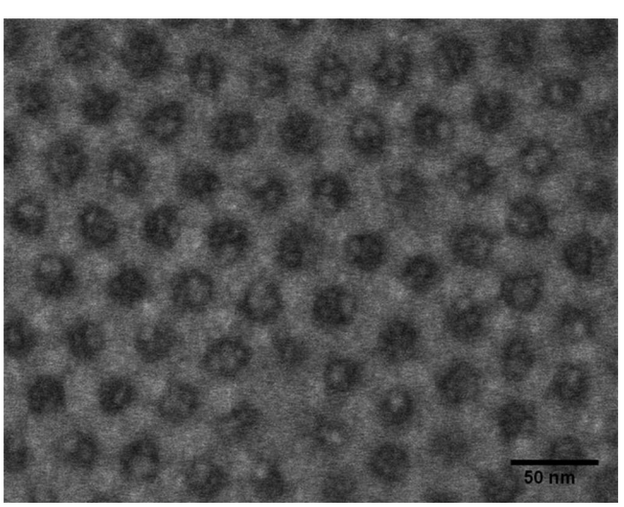

Figure 2. Plan-view SEM micrograph of CdSe NCs in nanopatterns after the second NC layer deposition.

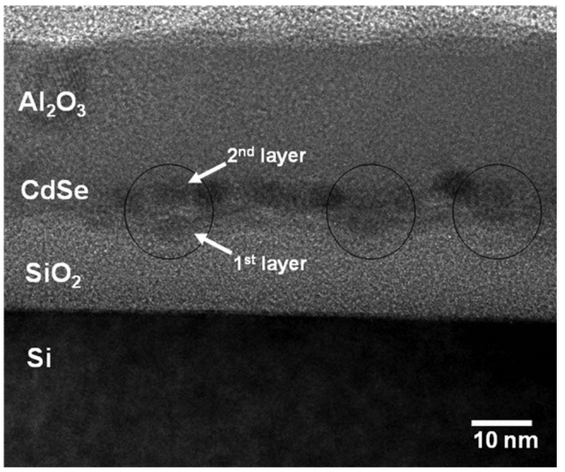

Figure 3. Cross-sectional-view high resolution TEM micrograph of ALD-Al_2O_3(25 nm)/second-CdSe-NCs/ALD-Al_2O_3(2 nm)/first-CdSe-NCs/nanopatterned-SiO_2(15 nm)/p-Si substrate.

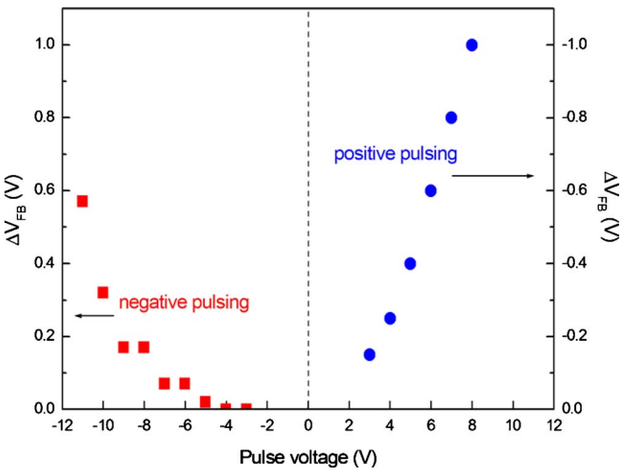

Figure 5. (Color online) ΔV_{FB} after applying positive and negative gate pulsing voltages for 10 s.

TOPO surfactant is 1.2 nm.[20] These van der Waals energies are comparable to or smaller than thermal energy at room temperature. Therefore, the NCs do not strongly attach on the top surface of SiO_2 and Al_2O_3 but can be driven into the nanopatterns. As a result, both the first and second nanocrystal layers could be deposited inside the patterns as vertically and laterally self-aligned double layer structures by the dip-coating process.

Figure 3 is the cross-sectional-view high resolution TEM micrograph of double layers of NCs embedded in dielectric layers. The thickness of the Al_2O_3 control oxide, Al_2O_3 interdielectric layer, and SiO_2 layer is ~25, 2, and 15 nm, respectively. Also, two layers of NCs are observed and some of them are clearly vertically aligned (marked with circles in Fig. 3). The observation of a rather irregular distribution of NCs is thought to originate from the overlapped imaging of NCs in TEM analysis. Both SEM and TEM images (Fig. 2 and 3) lead to the conclusion that the double layers of NCs are vertically self-aligned inside the nanopatterns.

The *C-V* characteristics of the device are shown in Fig. 4. A flatband voltage (V_{FB}) was not shifted at the sweeping gate voltage from −2 to +2 V. With increasing gate sweep voltage, the hysteresis is observed to result from the charging of NCs. The V_{FB} was negatively shifted during backward sweep, i.e., sweeping from (+) to (−) voltage, while it was not much shifted during forward sweep from (−) to (+) voltage. The NCs were positively charged through the hole transport from the Al gate to the valence band of NCs or the electron withdrawing from the conduction band of NCs to the Al gate when the positive voltage is applied to the gate.

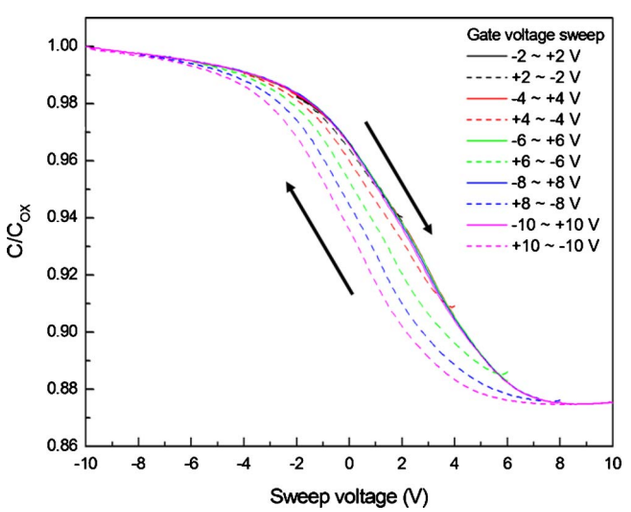

Figure 4. (Color online) *C-V* characteristics of the capacitor structure of Al-gate/ALD-Al_2O_3(25 nm)/second-CdSe-NCs/ALD-Al_2O_3(2 nm)/first-CdSe-NCs/nanopatterned-SiO_2(15 nm)/p-Si substrate.

The flatband voltage shift (ΔV_{FB}) after applying gate pulsing voltage for 10 s is shown in Fig. 5. The ΔV_{FB} was obtained from the *C-V* hysteresis curve in the range from −2 to 2 V after applying gate pulse voltage. The V_{FB} was negatively shifted after pulsing positive voltage. It implies the positive charging of NCs. As the positive pulsing voltage is increased, the magnitude of ΔV_{FB} increased negatively up to about −1 V at +8 V of pulsing voltage. For the double layer NC structure, the ΔV_{FB} is obtained by the contribution of charges at each layer, as shown in Eq. 1

$$\Delta V_{FB} = -\frac{1}{\varepsilon_{Al_2O_3}\varepsilon_0}(Q_{\text{first layer}} \times t_{\text{first}} + Q_{\text{second layer}} \times t_{\text{second}}) \quad [1]$$

where $\varepsilon_{Al_2O_3}$ is the relative dielectric constant of Al_2O_3 (calculated to be ~10.2 from the *C-V* curve) and ε_0 is the permittivity of free space; $Q_{\text{first layer}}$ and $Q_{\text{second layer}}$ are the charge density at the first and second layers of NCs, respectively, while t_{first} (32 nm) and t_{second} (25 nm) are the distance between the gate and each NC layer, respectively. If assuming the same charge density at the first and second layers of NCs, the total positive charge density is calculated to be $\sim 2 \times 10^{12}$ cm^{-2}. Because the nanopattern density is $\sim 7 \times 10^{10}$ cm^{-2} and each pattern has around five NCs on average,[10] the total NC density is $\sim 3.5 \times 10^{11}$ cm^{-2} if each layer has the same NC density. Thus, the number of charges in each NC is estimated to be about three at +8 V pulsing voltage.

The V_{FB} increased positively due to the electron transport from the Al gate to NCs through the Al_2O_3 control oxide when the negative pulsing voltage was applied to the Al gate. If the electron charging occurs as a result of Fowler–Nordheim (FN) tunneling, the electron charging from the Al gate to NCs can be understood by the lower electron tunneling barrier height (conduction band offset) between the Al gate and Al_2O_3 (~2.8 eV) than that between the Si substrate and SiO_2 (3.5 eV).[21,22] The magnitude of ΔV_{FB} by electron charging is ~0.17 V at −8 V of pulsing voltage, which is about 6 times smaller than that of positively charging at the same positive pulsing voltage. The positive charging of NCs is more efficient than electron charging in this structure. If the charging of NCs occurs

through FN tunneling, the energy barrier height for hole tunneling from Al to NCs or electron withdrawing from NCs to Al is lower than that for electron tunneling from Al to NCs. However, the values for barrier heights such as the conduction and valence band offset of $CdSe/Al_2O_3$ are not elucidated yet; hence, further investigation is necessary.

In addition, the optimization of device structure such as utilizing a bilayered tunneling oxide, nanocrystals having a high work function and improving the dielectric strength for the retention properties, and employing a metal gate with a higher work function is under investigation to fully utilize the advantage of the vertical and lateral self-alignment of NCs.

In summary, the vertically and laterally self-aligned double layer of NCs was formed by repeating selective deposition of colloidal NCs into nanopatterns and inserting ALD-Al_2O_3 dielectric layer between two layers of NCs. The selective deposition of colloidal NCs was achieved by the dip-coating process, during which NCs migrated into nanopatterns by capillary force. The charging of NCs was observed by the charge transport between the Al gate and NCs in the capacitor structure of the Al-gate/Al_2O_3(25 nm)/second-CdSe-NCs/Al_2O_3(2 nm)/first-CdSe-NCs/nanopatterned-SiO_2(15 nm)/p-Si substrate. The ΔV_{FB} of about -1 V at a programming voltage of +8 V for 10 s and about +0.57 at -11 V was achieved as a result of positively and negatively charging NCs. It demonstrates the formation of both vertically and laterally self-aligned NC double layers for the application to NC floating gate memory devices.

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