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Characterization of charging effect of citrate-capped Au nanoparticle pentacene device

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ABSTRACT

Capacitance–voltage hysteresis for a non-volatile memory was realized in a metal–pentacene–insulator–silicon (MPIS) device using gold (Au) nanoparticles (NPs) intervened between pentacene and SiO_2 insulator. A memory window higher than 2.0 V was obtained under (±) 5 V programming sweeping range. The SiO_2 as thick as 30 nm was adopted as the dielectric layer, and 3-aminopropyl-triethoxysilane (APTES) was used for self-assembling of Au NPs monolayer. In addition, citrate-functionalized Au NPs was dip-coated and used as charge storage elements. Formation of a monolayer of the Au NPs was confirmed by HR-SEM and AFM. Capacitance–voltage hysteresis in this study was resulted from the charge storage in the layer of Au NPs.

1. Introduction

Recently, a number of efforts have been introduced to fabricate memory devices based on organic materials and nanoparticles (NPs) [1–3,6,7]. The advantageous cost-effective non-volatile memory devices should be developed for large area electronics, low-cost dispensable sensor arrays, and memory tags. Their fabrication methods include trilayers having two intervening semiconductors' layers, an insulating organic layer with a middle metal layer, or polymeric blend of metal NPs [1–3]. Even organic light emitting bistable devices (OLEBDs) were successfully introduced for a dual functional device [9].

Semiconductors or metals for NPs are now an intense focus of research enabling their physical properties tailored for particular applications [6,7,8]. For example, an optical-induced charge transfer between semiconductor NPs and polymer layer has been applicable to solar cell devices. In addition, charge transfer on metal or semiconductor NPs has gathered much attention [2]. Especially, in organic or polymeric memory devices, an electric-field-induced charge transfer between Au NPs and the conjugated organic molecule has been a basic mechanism for memory effect [1,2]. In fact, the detailed mechanism of the electric-field-induced charge transfer should be related to the chemical structure of the capping or surfactant molecules on Au NPs. For the organic memory devices, current hysteresis appeared at the *I–V* measurement. The current in the second scan was significantly changed than the first one. These transitions were observed in air or under vacuum [1,2]. For some applications, a write-once-read-many time memory based on organic device could be obtained [2].

However, the mechanism of electric-field-induced charge transfer has been suspected with drawbacks induced by the metal deposition on top of the active organic layer [3]. It has been reported that the switching effects could be due to the formation or breaking of metallic nano-filaments rather than induced by electrostatic effects due to charge/discharge of NPs [3,4]. Bozano et al. proposed that an electroformed metal–insulator–metal diode is same to the organic device [3]. It was described that the electroforming process moves gold atoms from the electrode into the SiO_2 layer where they form an impurity band of charge transport levels, as well as deeper charge-trapping levels [3]. They used aluminum tris(8-hydroxyquinoline) (Alq_3) as the semiconductor, granular aluminum for the charge-trapping sites, and aluminum electrodes [3]. Alternative proposal invoked the formation of gold filaments to provide low-resistance pathways between electrodes [4]. By using heat-sensitive camera, it was shown that the conduction in the on-state is due to the presence of conducting paths through the bulk of the semiconductor. Their result suggested that switching is due to the oxide layer at the electrode and transport through filament [4].

For microelectronic applications, the 1–20 nm size of NPs can allow high device density. Au NPs can be deposited by Langmuir–Blodgett method or self-assembly [5,6]. Floating gate fabricated

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with Si or Ge nanocrystals have been introduced through the use of various techniques or ion beam synthesis [5]. Or, naphthalenethiol capped gold (Au) nanoparticle was attached on oxide by formation effect of self-assembled monolayer, then organic semiconductor, pentacene, was deposited. After deposition of the pentacene, electrode was formed by evaporation [6]. The fabrication scheme prevents gold atoms in Au NPs which does not have enough time or energy from diffusing into electrode. At the same time, the structure prohibits any possible formation of nano-filament from electrode to nanoparticle, since the thickness of pentacene is substantial, 60 nm. Frequency dependence existed with interface traps or did not exist with the Au NPs [6]. The device had a very thin dielectric oxide of 4.5 nm, which could be dependent on tunneling mechanism.

Here, we fabricated and characterized MPIS device having 30 nm thick oxide to prevent from any possible diffusion of gold atoms at top electrode into SiO_2.

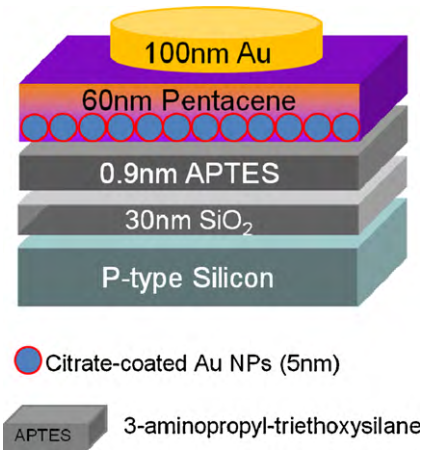

Fig. 1. A schematic diagram of MPIS (metal–pentacene–insulator–Si) capacitor device.

2. Experimental

Au NPs was purchased from British Bio Cell International (B.B.I.) (model: #EM.GC5/4). The gold colloid was of nominal diameter 5 nm in H_2O without any passivation. An aqueous 1 M citrate solution and gold colloid was mixed together at ratio of 1:1 in a 1.5 ml microcentrifuge tube and incubated for 24 h at room temperature. Then, the mixed solution was centrifuged in order to collect selectively citrate-coated Au NPs removing the remaining citrate molecules with filtration microcentrifuge tube (vivaspin 500, Cole Palmer, USA). The filtered citrate-coated Au NPs was suspended in deionized water. For fabrication of metal–pentacene–insulator–silicon (MPIS) structure, 30 nm thick thermal grown SiO_2 is formed on p-type silicon wafer, boron doped (1 0 0) silicon wafer having a resistivity of 10–15 Ω-cm. The substrate surface was first functionalized with 3-aminopropyl-triethoxysilane (APTES) by immersing the silicon wafer in 5 wt% volume of APTES in absolute ethanol for 1 h. The citrate-coated Au NPs were assembled on the amino-terminated silicon wafer by immersing the substrates into the citrate-coated Au colloid solution for 12 h at pH 6. After the deposition of the citrate-coated Au NPs, a 60 nm thick layer of pentacene and top gold electrode (1.0 mm radius size) are then deposited via sequential thermal evaporation. The thickness of gold electrode was 100 nm. An alphastep (KLA-tencor, U.S.A.) was used for the thickness measurement. Binding of the citrate-functionalized Au NPs on the APTES-coated SiO_2 surface was analyzed AFM (Park systems XE-100, Korea). SEM images for monolayered Au NPs were obtained with FESEM (JEOL JSM7000F, Japan) with magnification of 250,000. Capacitance–voltage measurements were performed by HP 4280A and Agilent 4284A LCR meter at the frequency of 1 MHz.

3. Results and discussions

Fig. 1 shows a schematic diagram of MPIS capacitor device. The self-assembled monolayer of APTES was introduced with an ability to produce uniform and stable adsorption of Au NPs on SiO_2 or Si substrates by electrostatic attraction between negatively charged citrate-coated Au NPs and positively charged amino terminating group ($-NH_2$) [6]. Gold electrode at top was adopted to ensure an efficient current injection into pentacene layer.

Fig. 2 shows AFM images of the self-assembled monolayer of Au NPs (a) on APTES functionalized SiO_2 surface and (b) on bare SiO_2 surface. The AFM result in Fig. 2(a) shows an uneven layer of Au NPs on the APTES-coated surface was formed. Therefore, the monolayered Au NPs were partially agglomerated. The rms of surface roughness was measured as 0.511 nm. In Fig. 2(b), it was easily found that there was no efficient surface binding of Au NPs on the bare SiO_2 surface.

Fig. 3 shows FESEM image of monolayer-coated Au NPs on APTES-coated oxide surface. In Fig. 3, along with the AFM analysis in Fig. 2(a), the partial agglomerations of the Au NPs were also detected. The empty regions formed by the agglomerated particles will be a source of defects in its capacitor device. With the SEM image, individual Au NPs could be counted in a limited area. It shows that average number of spatial density of coated Au NPs was

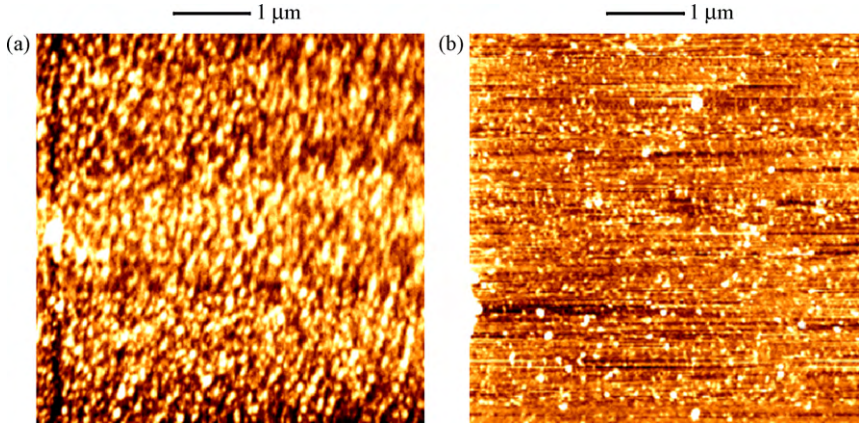

Fig. 2. AFM images of the self-assembled monolayer of Au NPs (a) on APTES functionalized SiO_2 surface and (b) on bare SiO_2 surface.

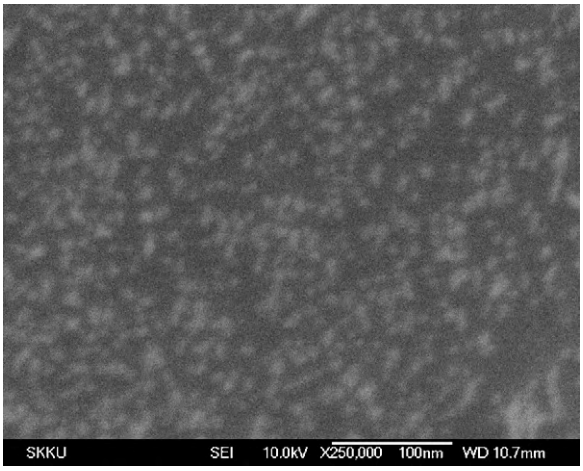

Fig. 3. FESEM image of monolayer-coated Au NPs on APTES-coated oxide surface.

$4.0 \times 10^{11}/cm^2$ with standard deviation of $8.2 \times 10^{10}/cm^2$. Since charging effect is expected from the individual Au NPs, the approximate counting and calculation of the particles' bindings can be correlated with the resultant performance of the device.

Fig. 4 shows the *C–V* results obtained from three different types of devices. The voltage was referenced from the top electrode. In Fig. 4(a), a control device without both Au NPs and pentacene layers (metal/APTES-coated SiO_2/Si) was characterized. Fig. 4(b) shows *C–V* behavior of another control device without Au NPs layer (metal/pentacene/APTES-coated SiO_2/Si). Fig. 4(c) shows a full device's *C–V* hysteresis (metal/pentacene/citrate-capped Au NPs/APTES-coated SiO_2/Si). With sequential double sweeps of *C–V* measurements, hysteresis behaviors by flatband-voltage shift could be detected. Fig. 4(a) shows there was no noticeable hysteresis detected regardless of sweeping direction. It shows there was no intentional charge trapping in the control device without Au NPs and pentacene. However, it is shown that highly contented negative fixed charges inside of the 30 nm oxide and poor interface contacts between the Au electrode and the APTES-coated SiO_2 resulted in a positive shift of flatband-voltage in Fig. 4(a) [10]. Fig. 4(b) shows *C–V* curves of the second control device which does not have Au NPs layer. Since there is the 60 nm pentacene layer, whose dielectric constant is similar to that of the SiO_2, in the second control device, the positive flatband-voltage shift observed in Fig. 4(a) was drastically reduced.

In Fig. 4(c), a *C–V* hysteresis window of 2.2 V in the full device was detected with sweep range of (±) 5 V. However, the slope of *C–V* at the depletion region in Fig. 4(c) was found to be lower than the slope of that in Fig. 4(b). The change of *C–V* slope is known to be originated from interface trapped charges [10]. Therefore, the introduction of the Au NPs itself or process of the Au NPs binding are believed to form the interface trapped charge. In addition, the origin of the hysteresis is also typically caused by the ion migration along with polarization of dipoles and injection of charges from electrode or Si [10]. Therefore, the origin of the hysteresis can be from both the ion migration and the charging effect of the Au NPs in this experiment.

When top electrode is positively biased, the positive charge density should increase at the pentacene/SiO_2 interface and the *C–V* curve should shift to the negative bias. Therefore, a clockwise hysteresis is observed, which indicates a hole trapping effect of the Au NPs.

In separate *C–V* measurements with high range of bias sweep, for example (±) 7 V, the hysteresis windows could be bigger than the 2.2 V. However, more declined slope of *C–V* was observed, which can

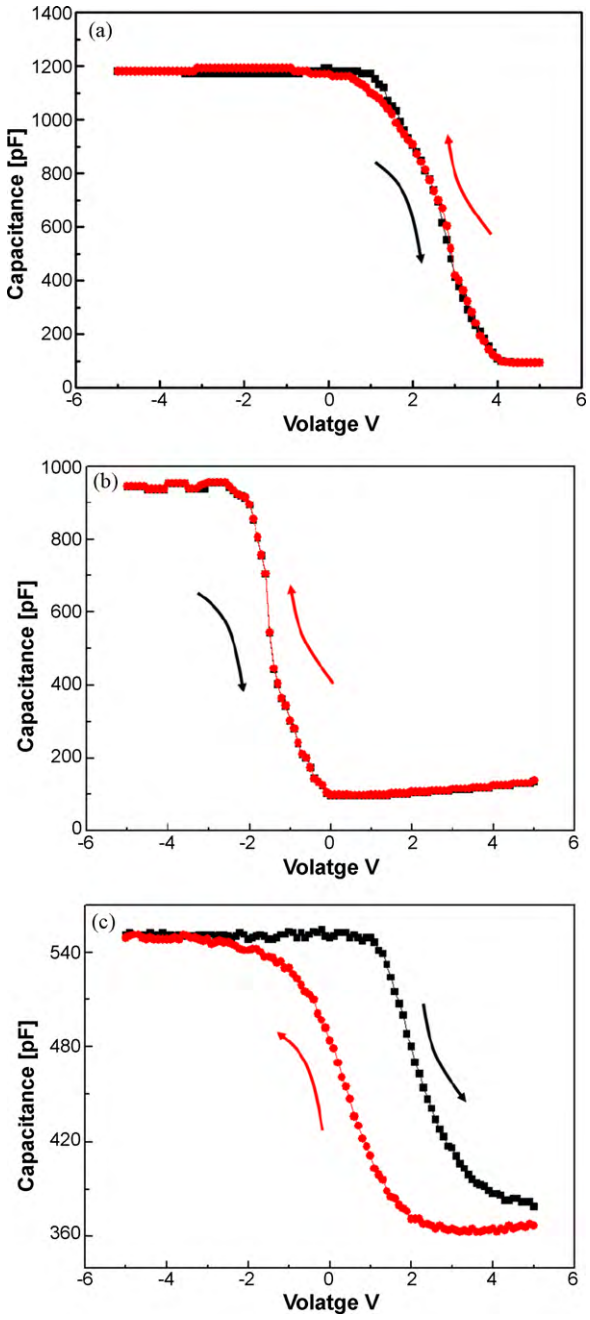

Fig. 4. *C–V* results (a) a control device without both Au NPs and pentacene layers (metal/APTES-coated SiO_2/Si), (b) another control device without Au NPs layer (metal/pentacene/APTES-coated SiO_2/Si) and (c) a full device (metal/pentacene/citrate-capped Au NPs/APTES-coated SiO_2/Si).

be an index of degradation of organic layers (data not shown). More detailed work and analysis on cycling stability and data retention times are also required in the future research.

4. Conclusions

The fabrication of organic memory capacitor using functionalized Au NPs has been demonstrated. The sweeping *C–V* characteristics of the device were shown to exhibit a hysteresis, which indicates a net charge trapping effect in the Au NPs. This approach, by virtue of its simplicity in fabrication processing, can realize integrated memory devices and circuits in low-cost plastic electronic applications.

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