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Selective Incorporation of Colloidal Nanocrystals in Nanopatterned SiO_2 Layer for Nanocrystal Memory Device

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CdSe colloidal nanocrystals with a size of ~5 nm were selectively incorporated in SiO_2 nanopatterns formed by a self-assembled diblock copolymer patterning through a simple dip-coating process. The selective incorporation was achieved by capillary force, which drives the nanocrystals into the patterns during solvent evaporation in dip-coating. The capacitor structures of an Al-gate/atomic layer deposition–Al_2O_3 (27 nm)/CdSe (5 nm)/patterned SiO_2 (25 nm)/p-Si substrate were fabricated to characterize the charging/discharging behavior for a memory device. The flatband voltage shift was observed by a charge transport between the gate and the nanocrystals. It demonstrates the colloidal nanocrystal application to a memory device through selective incorporation in regularly ordered nanopatterns by a simple dip-coating process.
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Memory devices with nanocrystals (NCs) embedded in a gate dielectric layer have been actively investigated for their improved scalability and retention properties, which also render a possible low voltage operation, thanks to the structure having discrete charge storage nodes.[1-3] To form isolated NCs embedded in a dielectric layer, various approaches have been employed, including thin-film deposition by chemical vapor deposition,[4,5] atomic layer deposition (ALD),[6] and physical vapor deposition,[7] during which NCs are formed at the nucleation stage of thin films. Also, ion implantation and subsequent annealing for precipitation of NCs [8] and oxidation of SiGe for Ge-rich NC formation[9,10] have been reported.

Though NCs can be successfully formed within a dielectric layer via the above-mentioned approaches, it is still challenging to achieve a uniform array of NCs with identical sizes and densities, which is crucial to realizing a uniform device performance. To this end, nanopatterning with a self-assembled diblock copolymer has been employed, where NCs are selectively formed in the patterns.[11,12] Black et al.[11] used a poly(styrene-*b*-methylmethacrylate) (PS-*b*-PMMA) diblock copolymer as an etching mask of a SiO_2 tunneling layer and subsequently formed Si NCs by chemical vapor deposition and an etch-back process, which left the Si NCs only inside the patterns as being isolated from each other. Also, Shahrjerdi et al.[12] used the same PS-*b*-PMMA diblock copolymer to pattern a structure of SiO_2/polyimide/SiO_2 multilayers for a lift-off process. Through the evaporation of Ni and a subsequent lift-off process by dissolving polyimide to remove the Ni layer on top of the SiO_2 layer, Ni NCs were finally left on the bottom of the SiO_2 patterns as being replicated from the diblock copolymer pattern. This selective formation of NCs on nanopatterns is a straightforward method to form the uniform array of NCs.

In this study, we employed the nanopattering of a SiO_2 dielectric layer with a self-assembled PS-*b*-PMMA diblock copolymer and selectively filled the patterns with colloidal CdSe NCs by a dip-coating process. This is a very simple process that consists of the patterning of a tunneling dielectric layer and subsequent dip-coating. Also, the structures, having single or multiple layers of various NCs, can be easily constructed through dip-coating with various colloidal NC solutions.

Thin films of the PS-*b*-PMMA diblock copolymer were used for the patterning of the SiO_2 layer with a thickness of 25 nm on a p-Si substrate. Before coating PS-*b*-PMMA, a polymer brush layer with a thickness of 5 nm was coated to induce the cylindrical microdomains oriented normal to the surface with a hexagonal pattern. Then, a 30 nm thick PS-*b*-PMMA layer was spin-coated and annealed at 170°C for 24 h to form the hexagonally self-assembled cylindrical patterns.[13] The copolymer pattern was transferred to the underlying SiO_2 layer by selectively removing the PMMA block and by reactive ion etching of the SiO_2 layer. The etched hole patterns have a diameter of about 20 nm with an ~40 nm center-to-center distance, which corresponds to a pattern density of 7×10^{10} cm^{-2}. The substrates were dipped into a CdSe colloidal NC solution, were withdrawn with a speed of 0.01 mm/s after a duration time of 1 min in the solution, and were dried in air at room temperature to deliver NCs into the patterns. The CdSe NCs with a diameter of approximately 5 nm, coated with a thin ZnS layer and trioctylphosphine oxide (TOPO) as a surfactant, were used as purchased from Nanosquare Inc. The CdSe NC had a composition of Cd:Se = 6:4, and the overcoating ZnS layer had a composition of Zn:S = 7:3, which were analyzed using inductively coupled plasma atomic emission spectroscopy. The NCs were dispersed in octane with a concentration of an order of 10^{16}/mL. The selective deposition of NCs inside the patterns was analyzed using scanning electron microscopy (SEM, Carl Zeiss LEO SUPRA 55) and transmission electron microscopy (TEM, JEOL JEM-3000F). For a clear observation of NCs, a high angle annular dark field (HAADF) imaging technique was also used for the TEM analysis.

To characterize the charging and discharging behavior, the capacitor structure was fabricated by depositing a 27 nm thick Al_2O_3 layer by ALD after dip-coating for CdSe NC deposition. ALD-Al_2O_3 was deposited using trimethylaluminum and H_2O for 250 reaction cycles at 300°C. During the ALD of the Al_2O_3 layer, some remaining surfactants on the surface were expected to desorb because the surfactants attached on the colloidal NC surface were readily desorbed above 200°C.[14,15] Then, the top Al gate was formed with a 200 μm diameter through evaporation and patterning by optical lithography and wet etching processes. The charging and discharging behavior was analyzed using high frequency capacitance–voltage (*C-V*) characteristics with a maximum sweep voltage from −30 to 30 V and a frequency of 1 MHz with a 25 mV oscillation using an Agilent 4284A precision LCR meter. The procedure of the selective formation of NCs in nanopatterns and the device structure for the *C-V* analysis are schematically illustrated in Fig. 1.

Figure 2 is the plan-view SEM micrograph of CdSe NCs in SiO_2 hole patterns. The CdSe NCs are selectively incorporated into almost entire hole patterns. As previously reported, the colloidal NCs can be selectively deposited inside the patterns by the capillary-

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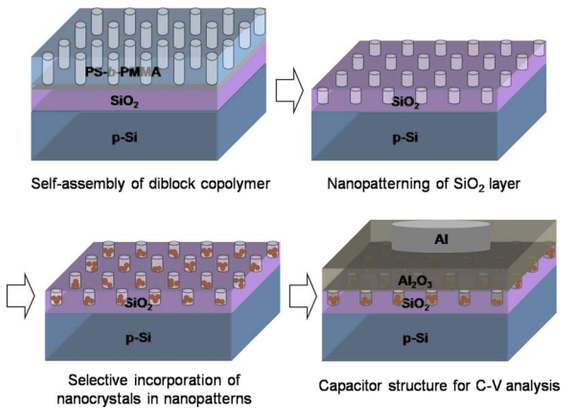

Figure 1. (Color online) Schematic illustration of the procedure of selective incorporation of NCs in nanopatterns and the device structure for the *C-V* analysis.

force-driven migration into the patterns.[16-18] During the solvent evaporation, while withdrawing the substrate from the solution, the capillary force operates at NCs at the edge of the solution interface with the patterned surface. This force with a direction into the patterns is ~80 kT/nm for NC with a 5 nm diameter, which is strong enough to drive NCs into the patterns selectively.[18] During dip-coating, NCs can adsorb on the top surface of SiO_2 by the van der Waals interaction.[19,20] The van der Waals interaction energy between CdSe, with a 5 nm diameter, and SiO_2 substrates across the medium of an octane solvent, with a distance of 1.2 nm by the TOPO surfactant, is calculated to be ~0.28 kT.[20] In this calculation, the Hamaker constants of CdSe, SiO_2, and octane are 0.388,[21] 0.41,[19] and 0.28 eV,[19] respectively, and the length of the TOPO surfactant is 1.2 nm.[22] The van der Waals interaction energy of 0.28 kT is weaker than the thermal energy at room temperature. Therefore, the NCs do not strongly attach on the SiO_2 top surface but are driven into the patterns by the capillary force upon solvent evaporation.

Figure 3 is the plan-view HAADF and cross-sectional bright-field (BF) and HAADF TEM micrographs. The plan-view image clearly shows the assemblies of several NCs forming clusters that are separated from each other. In accordance with the SEM image in Fig. 2, each cluster represents the NC assembly selectively formed at each isolated hole pattern even though the hole pattern image is not clear. The incorporation of NCs inside the hole is clearly verified in the cross-section image in Fig. 3b and c. Because the hole pattern is about four or five times larger than NC, about three to six NCs gather and form a cluster in a single hole pattern. However, the plan-view TEM image reveals that the NCs do not form perfectly

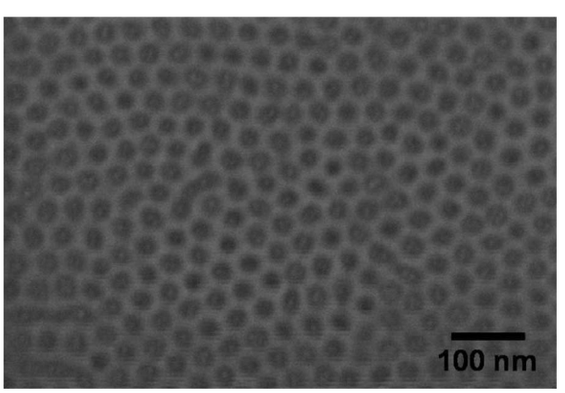

Figure 2. Plan-view SEM micrograph of CdSe NCs in regularly ordered nanopatterns of the SiO_2 layer.

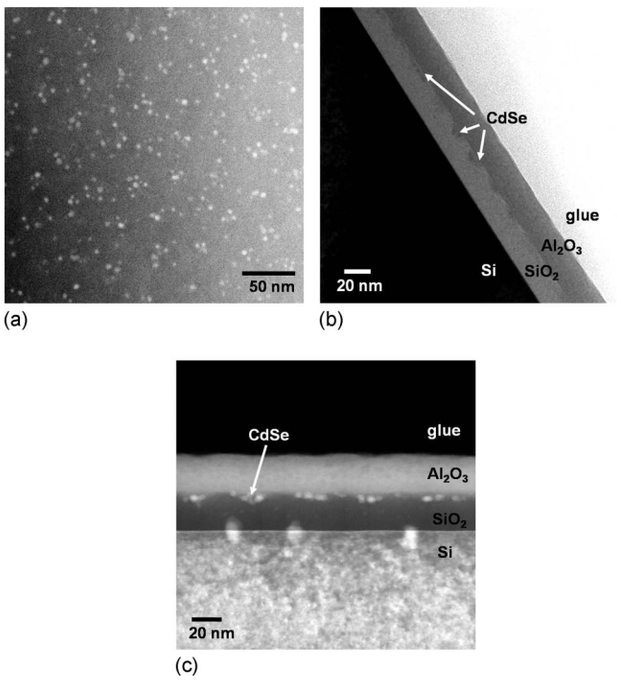

Figure 3. (a) Plan-view HAADF, (b) cross-sectional BF, and (c) cross-sectional HAADF TEM micrographs of CdSe NCs in nanopatterns of the SiO_2 layer.

ordered assemblies because the hole patterns are not formed as a long-range-ordered structure. Also, nonclose-packing of NCs in a cluster leads to the irregular distribution of NCs in patterns. These statistical distributions are thought to result in the irregular assembly structures. At the cross-sectional images, the thickness of SiO_2 and Al_2O_3 layers is measured to be about 25 and 27 nm, respectively, and the depth of the etched hole is about 5–10 nm. These results demonstrate the selective deposition of NCs inside the regularly ordered hole pattern with a simple dip-coating process. It provides the simple process scheme to integrate NCs into the device structures that can be further extended to those having multiple NC layers or heterostructure with various NCs integrated in a single device.

The *C-V* characteristics of the device are shown in Fig. 4. As a reference, the flatband voltage shift (ΔV_{FB}) was not observed in a control device without NCs, as shown in Fig. 4a. Also, the flatband voltage was not shifted when a gate voltage was swept from −10 to 10 V. As a sweeping gate voltage from −20 to +20 to −20 V (solid line) and from −30 to +30 to −30 V (dashed line), the *C-V* curve clearly shows the hysteresis (Fig. 4b). In contrast to a typical NC memory showing a positive shift of flatband voltage by electron tunneling from a Si substrate at the positive gate voltage, it shows that the flatband voltage is positively shifted during sweeping from the negative voltage. The positive shift at the negative gate voltage implies that electrons are transported from the top gate to NCs. These electrons are discharged during sweeping from the positive voltage. The magnitude of ΔV_{FB} is 4.6 V for −20/+20 V of sweep voltage and 8.4 V for −30/+30 V. These values correspond to the charge densities of 8.5×10^{12} and 1.5×10^{13} cm^{-2}, respectively, which are calculated with an Al_2O_3 dielectric constant of 9 and a thickness of 27 nm. Because the hole pattern density is about 7×10^{10} cm^{-2} and each hole has around five NCs on average, the total NC density is about 3.5×10^{11} cm^{-2}. Thus, each NC is charged by about 40 electrons at the −30/+30 V programming condition. In the structure with NCs embedded in a dielectric layer, the gate voltage for an electron charging in an NC is expressed as $e/2C$, where e is the magnitude of electron charge and C is the CdSe

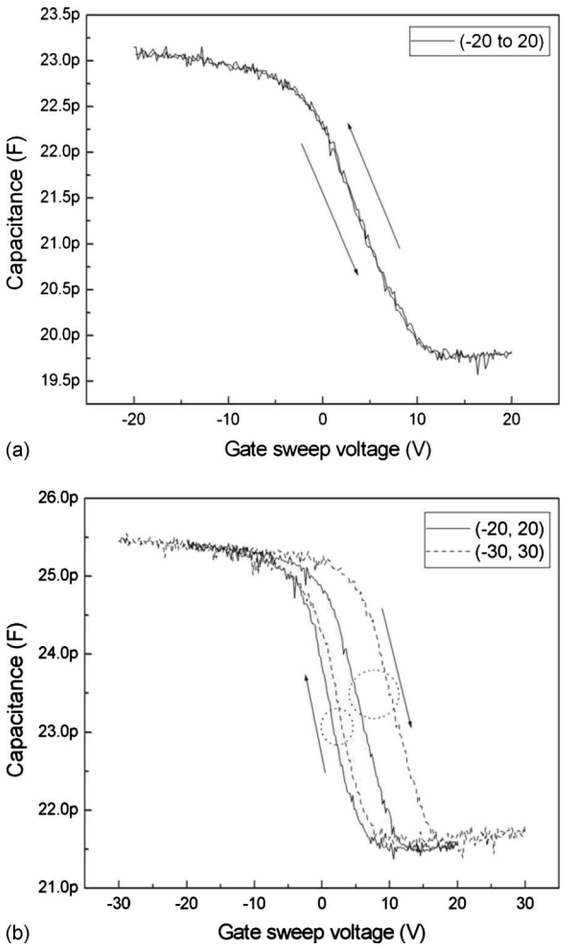

Figure 4. The *C-V* characteristic of the capacitor structure of (a) the Al-gate/ALD-Al_2O_3 (27 nm)/patterned SiO_2 (25 nm)/p-Si substrate without CdSe NCs and (b) the Al-gate/ALD-Al_2O_3 (27 nm)/CdSe (5 nm)/patterned SiO_2 (25 nm)/p-Si substrate with a gate voltage swept from −20 to +20 V (solid line) and from −30 to +30 V (dashed line).

$NC/SiO_2/Si$ substrate capacitance associated with a 5 nm diameter of NC when electrons are charged from the gate to the NC. The interval of the voltage for subsequent electron charging is e/C.[23] From these equations, the maximum number of electrons in an NC is ~10 at the gate voltage of −30 V, which is less than the experimentally measured one (40 electrons). This discrepancy is thought to be due to the traps generated from surfactants that were not completely desorbed and interfaced between NCs, and the surrounding dielectric layers store additional electrons. Therefore, the charge density can be higher than the calculated one. The charges in both NCs and trap sites can be utilized to obtain the memory characteristics. However, the charges stored in the traps with different energy levels may cause the deviation of the retention characteristic, which eventually limits the application to highly integrated devices. To clarify the effect of charges at trap sites, the study on the trap density, location, and their energy levels is further required.

The charging and discharging of NCs by the electron transport between the top gate and NCs are due to the similar thicknesses of the SiO_2 and Al_2O_3 control oxides (Fig. 3b), while a smaller conduction band offset is measured between the Al gate and Al_2O_3 (about 2 eV) compared to that measured between the Si substrate and SiO_2 (3.5 eV).[24,25] For the practical application compatible with the current flash memory operation, the tunneling of the charge should occur from the Si channel. Therefore, the device performance having a thinner tunneling oxide on the Si channel and the effect of traps associated with colloidal NCs should be further investigated.

In summary, uniformly self-aligned NCs could be obtained by a simple dip-coating of a nanopatterned substrate into a colloidal CdSe NC solution. The NCs were selectively incorporated into nanopatterns by the capillary force when the solvent evaporates during the dip-coating process. The charging and discharging of NCs by electrons and the resulting flatband voltage shift in the *C-V* analysis of the capacitor structure were observed. These behaviors demonstrate the application of colloidal NCs and the simple dip-coating process to selectively incorporate NCs in the nanopatterned tunneling dielectric layer for NC memory devices.

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