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Electrical Charging/Discharging Properties of Organic Memory Device Using CdSe Nanoparticles/PMMA Blend as the Tunneling Layer

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The electrical charging/discharging phenomena in organic memory based on the PMMA+CdSe nano-particles (NPs) blend tunneling insulator were demonstrated. The CdSe NPs multilayer could be easily fabricated by simple spin-coating process of blended solution of CdSe NPs in PMMA. Due to the hole trapping, the capacitance-voltage (*C-V*) characteristics exhibit a large counterclockwise hysteresis that is proportional to the gate bias sweep range. This simple fabrication method have a large memory window of 14.9 V after writing and erasing modes and a long charge retention ability over 10,000 s.
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Organic electronics have been studied with much interest over the last decade, due to their attractive features such as low cost, low temperature processing and mechanical flexibility.[1–3] Many applications such as organic solar cell,[4] organic thin film transistor,[5] organic circuit,[6] organic light emitting diode,[7] and organic sensor[8] are the focus of intense study. Besides, a high performance organic memory will be of a strong impact and several types of organic memory devices have been evaluated, including organic electrical bistable devices,[9] organic–inorganic hybrid memory[10] and organic field-effect transistors (OFETs) based on ferroelectric gate insulators,[11] chargeable gate dielectrics,[12] and nano-particles (NPs) floating gate organic memory device. The NPs floating gate organic memory is featured to have advantages low power consumption, small device size, excellent stress induced leakage current (SILC) immunity, and better retention from NPs-incorporated memory structures.[13,14] Most studies in this direction have focused on the metallic NPs such as Cr,[15] Ag,[16] and Au[17]) in the floating gate organic memory devices. On the other hand, semiconductor NPs possess many intriguing properties and are a powerful tool for the development and fabrication of materials with novel functions. Interestingly, when more than one types of such semiconductor NPs are placed at designated positions in electric devices, they can function as quantum dots having specific characteristics of individual material. Their fabrication methods include self-assembled monolayers of the NPs[18] and Langmuir-Blodgett films with intervening NPs between pentacene and dielectric.[19] However, these methods need complicated processes along with the repetitive NPs adsorption steps and NPs adhesion layer.

Therefore, in this study, we realized the NPs floating gate memory with CdSe NPs dispersed in PMMA insulating layer with much simplified procedure. The unique feature of this study is that the multilayer of CdSe NPs are formed inside the PMMA tunneling insulator, which provides a large memory window, potential multilevel charging characteristics, and improved retention properties. The NPs multilayer could be easily fabricated by simple spin-coating process of blended solution of CdSe NPS in PMMA.

The schematic of the bottom-gate memory device structure used in this work is shown in Fig. 1a. The metal-insulator-semiconductor (MIS) structure was fabricated on the indium tin oxide (ITO) glass substrate. The ITO layer was used as gate electrode. As a control device without CdSe NPs, PMMA (molecular weight 950 K, diluted in 4% anisole) as a gate insulator, was spin-coated twice at 4500 rpm for 60 s over ITO and subsequently baked at 160 °C for 30 min in a conventional oven. In this way, the thickness of PMMA layer was about 400 nm. For the NPs floating gate memory, the CdSe NPs solution (30 wt %) was mixed with PMMA solution. The CdSe NPs/PMMA layer (50 nm) was spin-coated on PMMA layer (200 nm) and subsequently baked at 160 °C for 30 min in a conventional oven to make PMMA gate insulator having homogeneously distributed CdSe NPs inside PMMA. The CdSe NPs with a diameter of approximately 5 nm, coated with a thin ZnS layer and trioctylphosphineoxide (TOPO) as a surfactant, were used as purchased from Nanosquare Inc. The CdSe NPs had a composition of Cd:Se = 6:4, and the over-coating ZnS layer had a composition of Zn:S = 7:3. The CdSe NPs were dispersed in octane at a concentration of 10^{16}/ml. The pentacene layer was deposited by thermal evaporation at a rate of 0.1 Å/s to a thickness of about 70 nm at a high vacuum of less than 5×10^{-6} Torr. A top metal electrode of gold was subsequently deposited by thermal evaporation through a shadow mask of 500 μm diameter size. The cross-sectional scanning transmission electron microscopy (STEM) image of a fabricated device shown in Fig. 1b indicated that CdSe NPs were in fact uniformly embedded in PMMA layers without aggregation through blending process. The electrical properties of devices were analyzed by capacitance-voltage (*C-V*) characteristics at room temperature in ambient air using Agilent 4284A at a frequency of 100 kHz.

Figure 2 shows the *C-V* curves with respect to the gate voltage (V_{GS}). When as shown in Fig. 2, V_{GS} was swept from +10 to −10 V and then back to +10 V, the hysteresis was not observed due to low electric field for charge tunneling. With increasing V_{GS}, the hystereses were observed. When the hysteresis in the range of +/−40 V is compared to the former, the *C-V* curve appears to have shifted in the negative direction, which indicates that NPs were positively charged due to applied negative V_{GS}. The negative shift during application of $-V_{GS}$ indicates that holes are transported from the pentacene layer to CdSe NPs or the electrons are withdrawn from CdSe NPs through PMMA in PMMA+CdSe NPs layer. The shift in the *C-V* curve, representing memory window, increased with increasing V_{GS} sweep due to higher charge injection. It should be noted that no such shift was observed when the gate voltage was swept from positive to negative direction. This indicates that positive charging of CdSe NPs was more efficient than their negative charging on this device. On the other hand, *C-V* analysis of a control device without CdSe NPs did not show the hysteresis when the gate voltage was swept in the same range (inset to Fig. 2). It indicated the density of charge trapping sites

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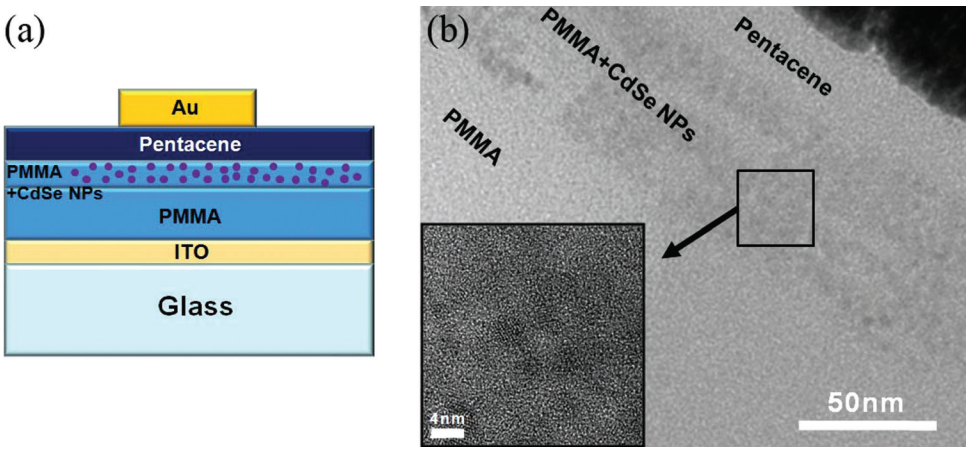

Figure 1. (Color online) (a) Schematic of the CdSe NPs/PMMA composition in the blend as the tunneling layer for non-volatile organic memory and (b) Cross-sectional STEM image of the fabricated device featuring CdSe NPs embedded in PMMA layer.

inside PMMA layer, while the PMMA-PMMA interface was negligible.

Figure 3 demonstrates the shift in *C-V* curve as a function of amplitude of the applied positive or negative gate voltage stress. The *C-V* curve shifted in negative direction when the V_{GS} of −30, −40, −50 and −60 V were applied for 2 s. On the other hand, it shifted slightly in positive direction after erasing the memory by application of a V_{GS} of +60 V for 2 s. The memory window (ΔV) after application of V_{GS} was measured with a capacitance of 6.6 pF/cm^2. The ΔV in this case was 2.7, 4.6, 8.3 and 14.9 V at V_{GS} of −30, −40, −50 and −60 V, respectively. Upon applying negative V_{GS}, the resultant negative ΔV was attributed to the positive charging of CdSe NPs. The positive charges on the CdSe NPs were rejected by application of positive V_{GS}, with an identical *C-V* sweep characteristic to Fig. 2. The charge density Q in CdSe NPs can be estimated from Q = CΔV, where C is the capacitance between gate and the CdSe NPs.[20] Since PMMA layer with CdSe NPs was deposited by spin-coating of mixed solution of CdSe NPs and PMMA, it is assumed that CdSe NPs were uniformly distributed in the PMMA layer. The charge density was calculated by further assumption that all the CdSe NPs were in the midst of PMMA layer. The charge density, Q, as calculated were 17.93×10^{10}, 30.54×10^{10}, 55.11×10^{10}, and 98.94×10^{10} #/cm^2 at the V_{GS} of −30, −40, −50, and −60 V, respectively, while assuming that each charge occupies one CdSe NP.

The charge retention characteristics of the devices were measured from the time-dependent capacitance change after programming at room temperature (Fig. 4). After programming with V_{GS} of −50 V for 2 s, the ΔC was measured at V_{GS} = 0 V by sweeping the gate voltage from 2 to −2 V in order to minimize the read disturbance. The capacitance was 6.961 nF/cm^2 after programming, which did not change even after 10^4 s, confirming that this device has the potential to be considered for non-volatile memory applications.

In summary, we demonstrated a CdSe NPs/polymer blend as the tunneling layer for non-volatile organic memory. The charging and discharging CdSe NPs were observed in the *C-V* analysis of MIS structure, showing the sufficiently large memory window and retention characteristics. This approach, by virtue of its simplicity in processing, can realize integrated organic memory devices in low-cost plastic electronics applications.

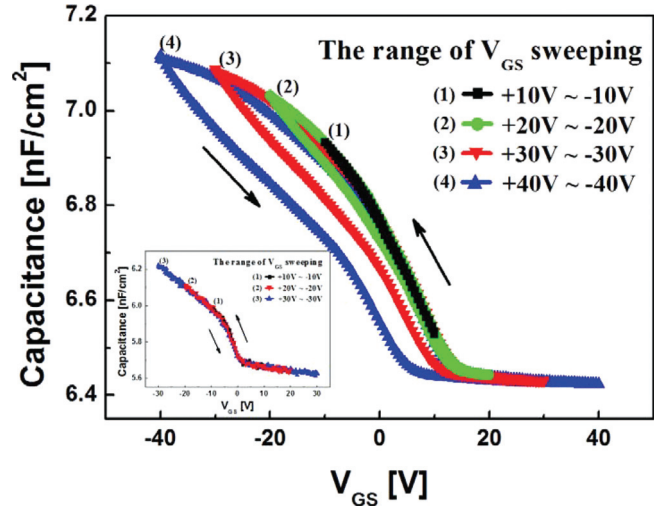

Figure 2. (Color online) The *C-V* characteristic of the fabricated organic memory at different V_{GS} sweeping range. The inset shows the *C-V* characteristic of a control device without CdSe NPs at different V_{GS} sweeping range.

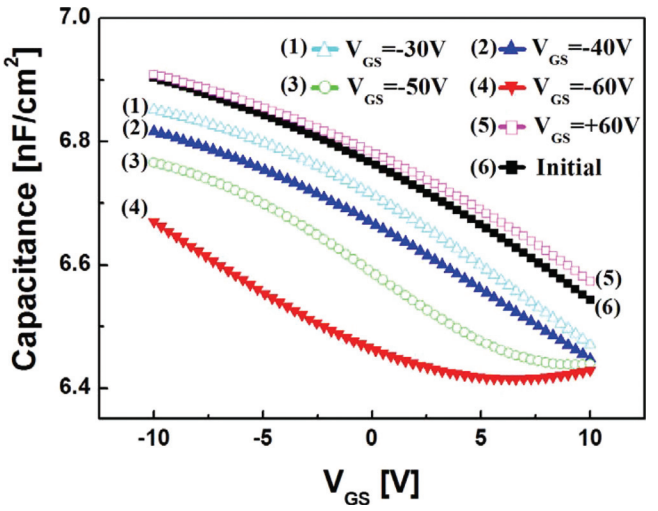

Figure 3. (Color online) Capacitance change (ΔC) as a function of the gate stress voltage for 2 s.

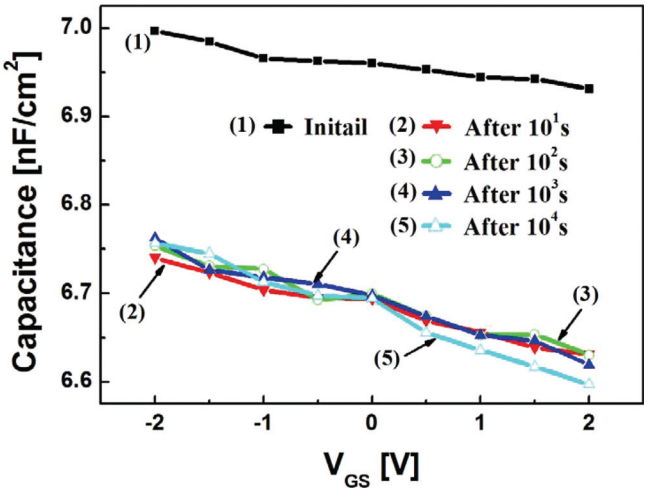

Figure 4. (Color online) Retention characteristics in terms of the capacitance after applying −50 V gate stress voltage for 2 s.

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