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Memory Charging Effect in Silicon Nanoparticles of Pentacene Capacitor Device

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In this study, an organic memory structure having citrate-capped silicon nanoparticles (Si NPs) self-assembled on SiO_2 layer is demonstrated to show memory charging effect. The Si NPs were prepared by a simple chemical oxidation and etching method with silicon powder. The hysteresis loops on *C–V* measurement were obtained by flatband voltage shifts, which demonstrate the presence of charge storages in the embedded pentacene capacitor of Si NPs. The formation of Si NPs and the citrate capping on the Si NPs were analyzed by high resolution transmission electron microscopy and Fourier transform infrared spectroscopy, respectively. With voltage sweep of $\pm$ 10 V, a hysteresis loop having flatband voltage shift of 9.9 V was obtained. In addition, electrical performance measurement for the charge storage showed more than 10,000 s charge retention time.
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Memory device structures containing semiconductor or metal nanoparticles (NPs) have received considerable attention due to their low operation voltage, fast write/erase speeds, and better endurance compared with conventional flash memory devices.[1–5] Particularly, NPs memory devices based on organic materials can be developed as an alternative solution over silicon (Si)-based device for the bendable or flexible electronics.[1–3] Even for the Si-based memory device, to overcome the scaling issue of electronic nonvolatile memories, the NPs can be an attractive charging element due to their nanoscale size.[6,7] However, so far, the precise control of NP layers to incorporate between gate dielectric layers has been an obstacle for a reliable device fabrication. Recently, there have been several reports about the successful formation of NP layers on SiO_2 substrate using the Langmuir–Blodgett film formation and self-assembly monolayer mechanism.[4,5,8–10] The mechanism to form the self-assembly monolayer is originated from an electrostatic force between the surface capped gold(Au) NPs with citrate and the activated SiO_2 surface with amine containing chemical.[8–10] The devices having the monolayered NPs have shown significant charging effect in the structure of capacitor. For the material of the charging NPs, metallic NPs have been widely reported, including Au, silver (Ag), platinum (Pt) NPs, etc.[6–11] The metal NPs such as Au, Ag, and Pt are advantageous due to their inertness to oxidition. However, the metal NPs having large workfunctions are potentially apt to reduce the injection efficiency of charge, especially for the organic devices.[4,5]

Typically, the method of formation of Si NPs can be categorized into bottom-up and top-down. The top-down method includes a production of Si NPs from crystalline or polycrystalline Si by an etching procedure to reduce the bulk Si. Even, the colloidal Si NPs having $\sim$1 nm size could be prepared by electrochemically etching process from Si bulk wafer.[12–14] The Si NPs were used as a luminescecnt element showing a single particle effect with oxide capping with H_2O_2 and HF. The oxide capping was turned out to reduce the quantum yield at 350 nm excitation and 390 nm emission.[13] Unlike the top-down process, the bottom-up process typically needs realtively complicated processes. For example, silane (SiH_4) pyrolysis using aerosol technique involves massive equipment including furnace and high-vacuum.[15] However, the controllability in shape and size of the Si NPs is adavantageous with the bottom-up process. In this study, the Si NPs were simply prepared out of Si powder from a sequential oxidation and etching process in aqueous solution of H_2O_2 and HF. Relatively narrow-dispersed Si NPs could be selectively recovered by the centrifugation and filtration process. The Si NPs were adopted as charging elements in a metal-pentacene-insulator-silicon (MPIS) capacitor device. The synthesized Si NPs were capped by citrate molecules, which can bind to amine group terminals of 3-aminopropyltriethoxysilane (APTES) by electrostatic force. Processing approaches for Si NP formation are addressed and corresponding memory device performances are discussed.

The Si NPs were fabricated by the chemical etching of oxidation and reduction. First, hydrofluoric acid, hydrogen peroxide, and methanol (1:1:1 vol%) were mixed with silicon powder (0.5wt%) in Teflon vessel at room temperature. Hydrofluoric acid (HF; 48 vol%) was purchased from J.T Baker and silicon powder was purchased from Alfa Aesar (silicon powder, crystalline, −325mesh 99.5%). Then, the mixed solution was incubated for 5min and centrifugated for 10 min. The supernatant after the centrifugation was taken and mixed with acetonitrile forming Si NP suspension. The red-brown supernatant having the Si NPs (diameter of 4–6 nm) was filtered by microcentrifuge tube (vivaspin 500, Cole Palmer, USA). The filtered Si NPs was dispersed in acetonitrile in order to minimize further oxidation. To fabricate the memory structure device, SiO_2 thermally grown to 10 nm on heavily doped P-type Si substrate [100] was adopted as a gate insulator. APTES (99%, Aldrich Chemistry) was deposited by dip-coating at 3.0 vol% solution with ethanol in order to immobilize amide group on SiO_2 surface. The Si NPs were capped by citric acid (1 M citrate solution) with mixing and incubation for 24 h. The mixture was centrifugated with filtration to collect selectively citrate-coated Si NPs removing the remaining citrate molecules. The collected citrate-capped Si NPs was suspended in deionized (DI) water. To form the self-assembled monolayer of the Si NPs, the APTES-coated substrate was immersed in the solution of citrate-capped Si NPs. To remove the unbound Si NPs on the surface of APTES, the device was rinsed in DI water for 30 min. Pentacene active layer and gold electrode of 0.5 mm diameter were deposited by thermal evaporator with 60 and 100 nm of thickness, respectively. The structure of the MPIS device and experimental details are also illustrated in Refs. 9 and 10. High resolution transmission electron spectroscopy (HRTEM) image of the Si NPs and selected area electron diffraction (SAED) were obtained by JEOL JEM 2100F microscope at an accelerating voltage of 200 keV. High resolution scanning electron microscopy (HRSEM) image was obtained by Philips XL30SFEG microscopy. *C–V* performance was measured by Agilent 4284A at 10 and 100 kHz of frequency. Retention test was performed by biasing 8 V to top electrode for 20 s and then *C–V* recoveries were measured with time.

Figure 1 shows a schematic diagram for the Si NP intervened MPIS device. Figure 2 shows HRTEM image (a) and (b) with inset image of SAED of the synthesized Si NPs. As shown in Fig. 2a, there were many Si NPs that were well dispersed. In addtion, there were no nanowires or nanorods as confirmed in the TEM image and most of Si NPs were spherical or round-shaped. From the TEM image in Fig. 2b, it is noticed that the Si NPs are in crystalline nature with inhomogeneous contrast within a single nanoparticle. The size of the Si NPs was relatively widely ranged within 3–9 nm in diameter, which also include elliptical shapes as well as spherical shapes. From the TEM image in Fig. 2b, it is noticed that the Si NPs

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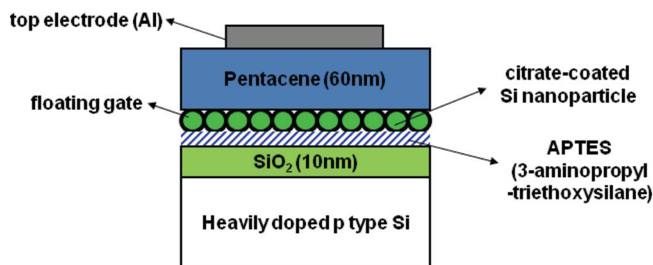

Figure 1. (Color online) Schematic diagram of Si NPs embedded MPIS device.

are in polycrystalline nature with inhomogeneous contrast within a single nanoparticle. In addtion, as shown in Fig. 2b, no apparent amorphous shells or SiO_2 shells were detected around the Si NPs.[15] We used SAED to characterize the crystalline structures of the NPs. The diffraction can be indexed to the (220), (311), (331), and (511)

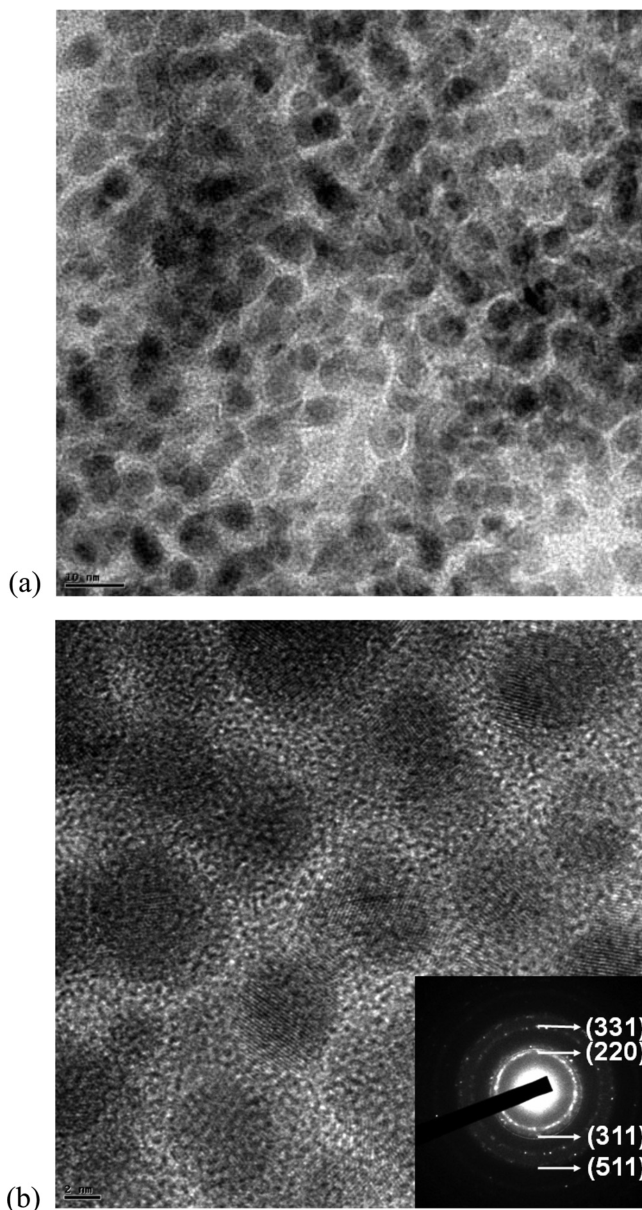

Figure 2. HRTEM image (a) and (b) with inset image of SAED of Si NPs prepared by oxidation and etching method.

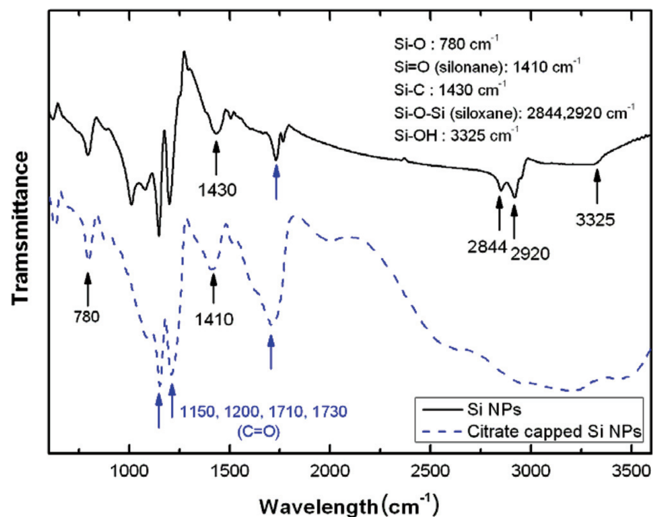

Figure 3. (Color online) FTIR spectra of bare Si NPs and citrate-capped Si NPs.

planes of crystalline silicon, respectively (JCPDS 27-1402). The electron diffraction (ED) rings were relatively broad due to the nature of polycrystalline structures as proven in the TEM image.

During the capping process of Si NPs with citrate, bindings of citrate on the Si NPs could be confirmed by Fourier transform infrared (FTIR) spectroscopy. Figure 3 shows the FTIR spectra of the Si NPs without capping and with citrate capping. In Fig. 3, both for the bare or uncapped Si NPs and the citrate-capped Si NPs, peak representing Si–O (780 cm^{-1}) and peaks representing C=O (1150, 1200, 1710, 1730 cm^{-1}) are commonly observed. Since the citrate molecule [$(C_3H_5O(COO)_3{}^{3-}$] has many carbonyl (C=O) groups, the spectrum for the citrate-capped Si NPs reasonably includes 1150, 1200, and 1710 cm^{-1} peaks. However, even though the bare Si NPs was dispersed in the acetonitrile (CH_3CN), many carbonyl peaks appeared as shown in Fig. 3. One possibility is that the C=O bond is from caboxylate ($O{=}C{-}O^-$) in solvent which is formed from dissolution of CO_2 gas in air. However, more investigations are needed to clarify this issue. In Fig. 3, for the uncapped Si NPs, unique peaks at 2844 and 2920 cm^{-1} pertained to siloxane(Si–O–Si) and at 3325 cm^{-1} pertained to Si–OH, which are shown.[12] However, after citrate capping as shown in Fig. 3, those peaks clearly disappeared, which proves successful capping of the Si NPs by citrate molecules. In

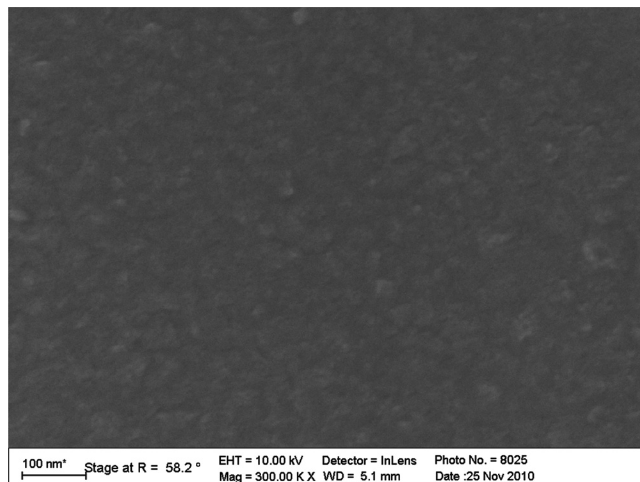

Figure 4. HRSEM image of monolayered Si NPs on APTES functionalized SiO_2 surface.

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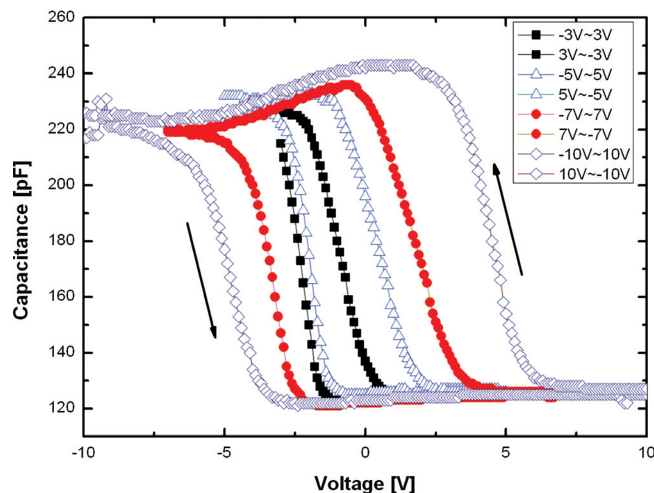

Figure 5. (Color online) Counterclockwise *C–V* characteristics of the memory device having 10-nm-thick SiO_2 with Si NPs layer at frequency of 100 kHz.

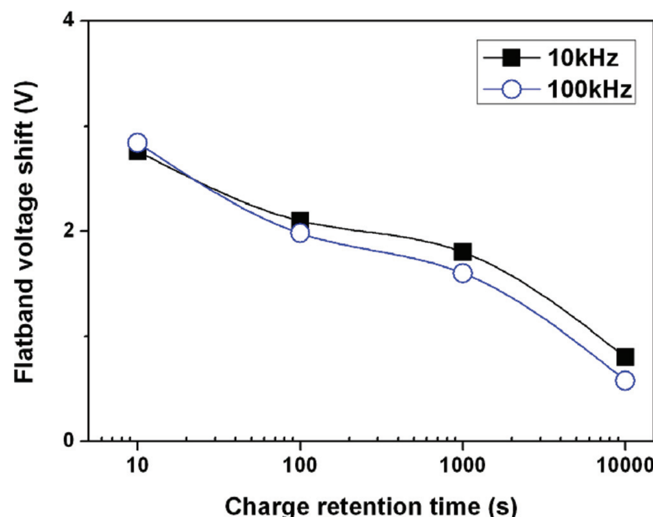

Figure 6. (Color online) Electrical retention test of Si NPs embedded MPIS device at frequencies of 10 and 100 kHz.

addition, the peaks of Si–O (780 cm^{-1}), Si–O–Si (2844, 2920 cm^{-1}), and Si=O (silonane: 1160, 1400 cm^{-1}) indicate that the surface of Si NPs are oxidized regardless of existence of capping.[12,13]

Figure 4 shows a HRSEM image showing the monolayered Si NPs on the APTES functionalized SiO_2 surface. Two-dimensional agglomerations of the flattened Si NPs were detected as reported in previous research with Au NPs.[9,10] It is shown that the Si NPs partially covered the APTES functionalized surface. The empty regions formed by the agglomerated particles will be a source of degradation of charging effect.[9] In this study, based on the SEM image, individual Si NPs could not be counted. As shown in Fig. 4, the monolayered Si NPs could not be identified individually due to their high density of electrostatically bound Si NPs and the wide size distribution of the Si NPs. However, Fig. 4 proves that the formation of Si NPs was not multilayered.

Figure 5 shows the *C–V* characteristics of the device at 100kHz frequency under different voltage sweep range. In a separate experiement, a control device without the intervention of Si NPs showed no hysteresis in the *C–V* characteristics.[9,10] As shown in Fig. 5, increase of voltage sweep range from ±3 to ±10 V increases the flatband voltage shift (ΔV_{FB}). The ΔV_{FB} for ±3 V range measured as 2.3V was increased to 9.9 for ±10 V range. The hysteresis loops are measured in counterclockwise direction, which indicates that leaky oxide (10 nm) formation at low oxidational condition or temperature may be one of the explanations.[4,5,10] As shown in Fig. 5, there were significant decreases of the capacitance in accumulation regions as the voltage into accumulation was increased. It is also known to originate from the ultrathin dielectric layer for capacitance measurement.[16]

Figure 6 shows the results of retention test for the charge storage of the Si NPs. The test was performed by biasing -8 V for 10 s at first, then, *C–V* measurements at the frequency of 10kHz and 100 kHz were executed sequentially after 10, 100, 1000, and 10,000 s after the bias. It was measured that the stored charge was retained upto 10,000 s. However, after 10,000 s, the *C–V* curves were converged into the 10,000 s *C–V* curve which is close to the original *C–V* behavior without the bias. As shown in Fig. 6, the higher frequency of *C–V* measurement was applied, the steeper the decrease of the charge retention was detected.[16]

In summary, the fabrication of organic memory device using Si NPs has been demonstrated. The sweeping *C–V* characteristics with the device were shown to exhibit hysteresis, which indicates net charge trapping effects in the Si NPs. In the *C–V* curves, the hysteresis loops are formed in a counterclockwise direction. These observations signify the injection and subsequent transfer of electrons stored in the NPs. In addition, flatband voltage shift increases with increase of sweep voltage range with the organic Si NPs memory device. Electrical performance for the charge storage shows the 10,000 s retention ability.

Acknowledgments

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