



Characterization of gold nanoparticle pentacene memory device with polymer dielectric layer

Hyung-Jun Kim^a, Sung Mok Jung^a, Yo-Han Kim^a, Bong-Jin Kim^a, Sanghyub Ha^a, Yong-Sang Kim^b, Tae-Sik Yoon^b, Hyun Ho Lee^{a,*}

^a Department of Chemical Engineering, Myongji University, Yongin-si, Gyeonggi-do, 449-728, Republic of Korea

^b Department of Nano Science & Engineering, Myongji University, Yongin-si, Gyeonggi-do, 449-728, Republic of Korea

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ABSTRACT

We report on the electrical behavior of gold nanoparticles (Au NPs) intervened metal-pentacene-insulator-semiconductor structures. The structure adopts polyvinyl alcohol (PVA) and pentacene as gate insulator and semiconductor, respectively. On the PVA (250 nm) film which was spin-coated and UV cross-linked, 3-aminopropyl triethoxysilane was functionalized for self assembling of the Au NPs monolayer. The devices exhibited clockwise hysteresis in their capacitance-voltage characteristics, with a memory window depending on the range of the voltage sweep. A relatively large memory window of about 4.7 V, which was deduced from control devices, was achieved with voltage sweep of $(-/+)$ 7 V. Formation of the monolayered Au NPs was confirmed by field effect scanning electron microscopy and atomic force microscopy.

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1. Introduction

Organic memory devices fabricated from metal-pentacene-insulator-semiconductor (MPIS) structures incorporating nanoparticles (NPs) as the charge-storage elements have been receiving considerable attentions recently [1,2]. Devices based on the organic materials such as pentacene have a potential to overcome many process problems associated with silicon structures. For example, organic materials can be deposited at room temperature on various surfaces including flexible substrates. Meanwhile, for complementary metal-oxide-semiconductor memory devices, different type of storage media have been introduced, such as aluminium (Al) nanocrystals (NCs) [3], gold (Au) NCs [4], Au NPs [5–7], and ferroelectric polymers [8,9]. Charging of the NCs or NPs occurs on the application of a voltage to the gate electrode by electron transport, either through a thin tunneling oxide [4] or the top insulator [2,6]. Some recent research has explored the use of high- k dielectrics for the formation of the tunneling oxide [5]. Except for the ferroelectric polymers, the NPs were incorporated into floating gate which is a charging layer on inorganic dielectric layers, such as SiO₂ and Al₂O₃.

Polymer materials have recently been applied as gate insulators because of their impressive improvement of the electrical performance and efficiency of organic materials [10,11]. Moreover, the attraction of plastic electronics based on the polymer materials is

driven by the possibility of enabling applications such as flexible and transparent electronic devices. Especially, polyvinyl alcohol (PVA) has been known as a promising candidate for a good gate insulator in the fabrication of organic thin film transistors [11,12]. It shows high dielectric constant ($\epsilon = 3.88$), good surface interfacing effect by rubbing [11], photosensitivity, and ability to be patterned by UV exposure [12]. In addition, the PVA has been studied due to benefits with water solvent and moisture inhibition by cross-linking from UV exposure forming a hexa-coordination of trivalent chromium with the help of PVA hydroxyl groups [13]. Cross-linked PVA chains result into a higher resistance gate dielectric that exhibit lower leakage currents [13,14].

Recently, possibility to form an organic memory device was demonstrated using the citrate-stabilized Au NPs as the charge storage components in a MPIS configuration [2]. In addition, the Langmuir-Blodgett deposition of organically passivated Au NPs which has been incorporated into a MIS structure is studied [1,7]. These experiments extend the understanding and applicability of charge trapping using monolayer of Au NPs.

In this paper, we reported on the formation of Au NPs monolayer at room temperature using a dip-coating process, and the memory effects of the Au NPs monolayered device were characterized from hysteresis of capacitance-voltage (C-V) measurement. The experimental procedure includes utilization of 5 nm Au NPs dip-coated on cross-linked PVA film, which has an binding layer of 3-aminopropyl triethoxysilane (APTES) on the PVA for the Au NPs. The C-V behaviors were compared among the Au/PVA/Si, Au/pentacene/APTES-coated PVA/Si, and Au/pentacene/Au NPs/APTES-coated PVA/Si structures.

* Corresponding author. Tel.: +82 31 330 6392; fax: +82 31 337 1920.
E-mail address: hyunho@mju.ac.kr (H.H. Lee).

2. Experimental details

Au NPs were purchased from British Bio Cell International (#EM. GC5/4). The Au colloid was in H₂O without any passivations. An aqueous 1 M citrate solution and gold colloid was mixed at volume ratio of 1:1 in a 1.5 ml microcentrifuge tube and incubated for 24 hrs at room temperature. Then, the mixed solution was centrifuged in order to collect selectively citrate-functionalized Au NPs discarding the remaining citrate molecules with filtration microcentrifuge tube (vivaspin 500, Cole Palmer). The filtered citrate-coated Au NPs were suspended in deionized water. For the fabrication of the MPIS structure, 250 nm thick PVA layer on p-type silicon wafer (boron doped (100) having a resistivity of 10–15 Ω-cm) was prepared by spin coating and sequential cross-linking by UV exposure. The PVA films in study were all cross-linked otherwise specified. The PVA surface was functionalized with APTES by immersing the substrate into 5 wt% of APTES in absolute ethanol for one hour. Then, the citrate-coated Au NPs were assembled on the amino-terminated PVA film by APTES through immersing the substrates into the citrate-coated Au colloid solution for 12 hrs at pH 6. After the monolayer deposition of the citrate-coated Au NPs, 60 nm thick layer of pentacene was deposited at a rate of 0.01 nm/s and 100 nm thick top gold electrode (1.0 mm radius) was sequentially deposited via thermal evaporation. An alphastep (KLA-tencor, U.S.A) was used for the thickness measurement. Binding of the citrate-functionalized Au NPs on the APTES-coated PVA surface was analyzed by atomic force microscopy (AFM: Park systems XE-100, Korea) in contact atomic force microscopy mode with a general cantilever. SEM images for monolayered Au NPs were obtained with field-emission scanning electron microscopy (FESEM: JEOL JSM7000F, Japan) at an accelerating voltage of 100 keV. C-V measurements were performed by Agilent 4284A LCR meter at the frequency of 1 MHz in air at room temperature.

3. Results and discussion

Fig. 1 shows a schematic diagram of MPIS capacitor device. The self-assembled monolayer of APTES was introduced for an ability to produce uniform and stable adsorption of Au NPs on PVA by electrostatic attraction between negatively charged citrate-coated Au NPs (COO⁻) and positively charged amino terminating group (NH₃⁺) [2,7]. Gold electrode at top was adopted to ensure an efficient current injection into pentacene layer [11].

Fig. 2 shows AFM images of the monolayered Au NPs (a) on APTES-functionalized PVA surface and (b) on bare PVA surface. The AFM result in Fig. 2(a) shows that an uneven layer of Au NPs on the APTES-coated surface was formed. Therefore, the Au NPs were believed to be partially agglomerated. The rms of surface roughness was measured as 0.508 nm. In Fig. 2(b), it was easily found that there was no efficient surface binding of Au NPs on the bare PVA surface.

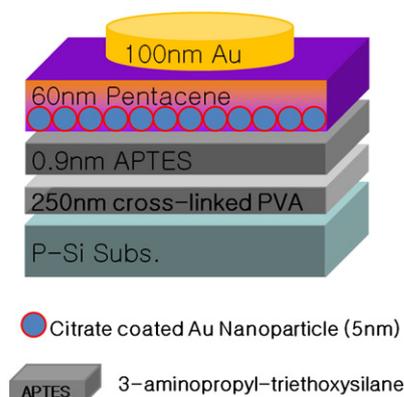


Fig. 1. A schematic diagram of MPIS (metal-pentacene-insulator-Si) capacitor device.

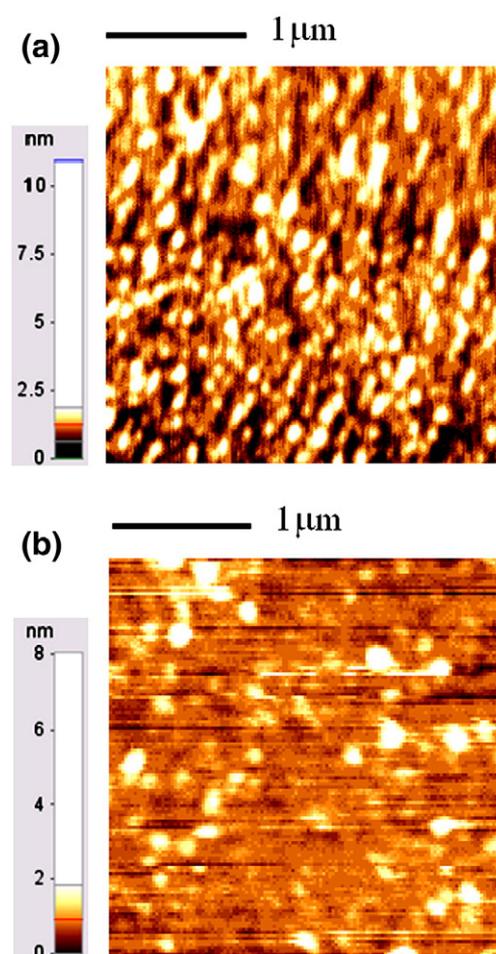


Fig. 2. AFM images of the self-assembled monolayer of Au NPs (a) on APTES-functionalized PVA surface and (b) on bare PVA surface.

Fig. 3 shows FESEM image of monolayer-coated Au NPs on APTES-coated PVA surface. In Fig. 3, along with the AFM analysis in Fig. 2(a), the partial agglomerations of the Au NPs were also detected but identified as two dimensional. The empty regions formed by the agglomerated particles will be a source of defects in its capacitor device. With the SEM images, individual Au NPs could be counted in a confined area. It shows that average number of spatial density of self-assembled Au NPs was $1.60 \times 10^{12} \text{ cm}^{-2}$ with standard deviation of $5.3 \times 10^{11} \text{ cm}^{-2}$. Since charging effect is expected from the individual

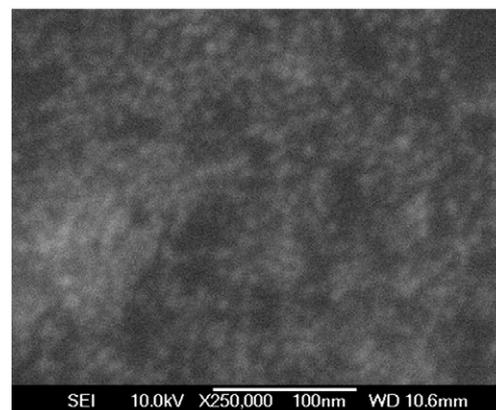


Fig. 3. FESEM image of monolayer-coated Au NPs on APTES-coated PVA surface.

Au NPs, the approximate counting and calculation of the NPs' bindings can be correlated with the consequential performance of the device.

Fig. 4 shows the C-V results obtained from three different types of devices. In Fig. 4(a), a control device without both Au NPs and pentacene layers (metal/PVA/Si) was characterized. Fig. 4(b) shows C-V behavior of another control device only without Au NPs layer

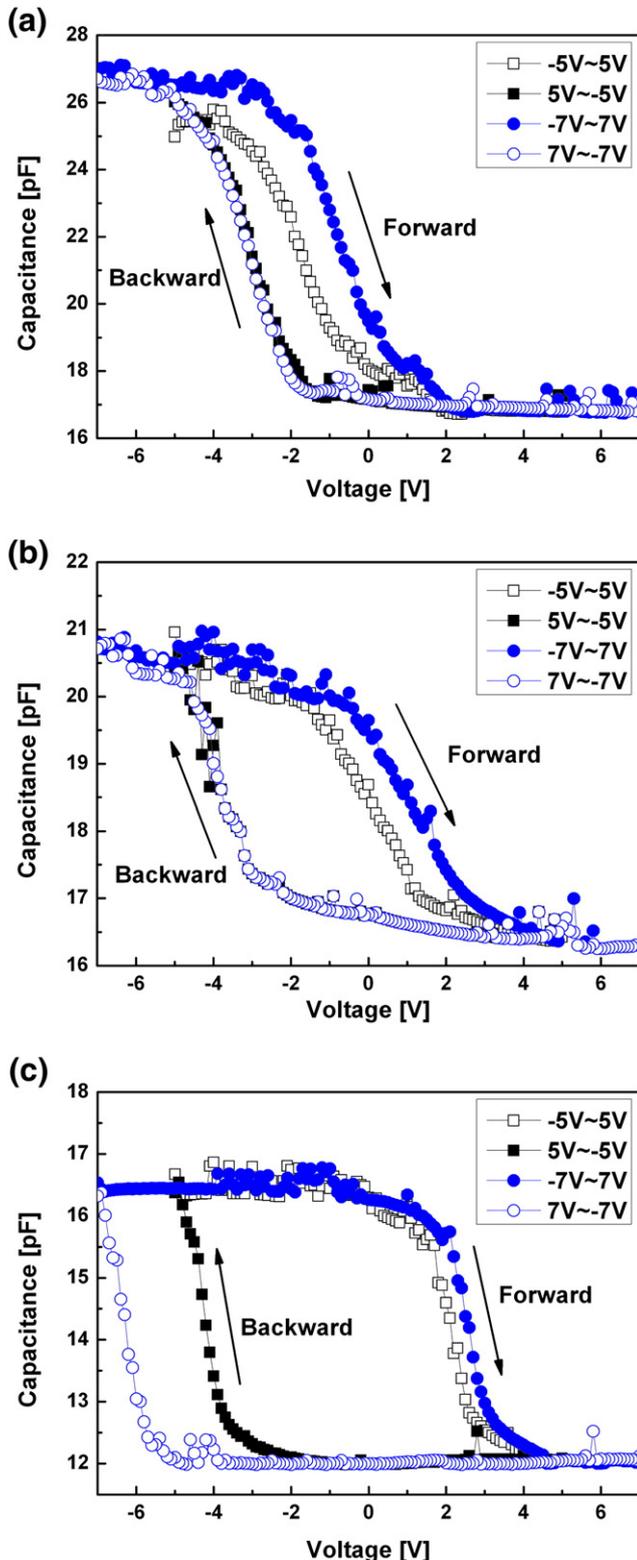


Fig. 4. C-V results (a) a control device (metal/PVA/Si), (b) another control device without Au NPs layer (metal/pentacene/APTES-coated PVA/Si), (c) a full device (metal/pentacene/citrate-capped Au NPs/APTES-coated PVA/Si).

(metal/pentacene/APTES-coated PVA/Si). Fig. 4(c) shows a full device's C-V hysteresis (metal/pentacene/Au NPs/APTES-coated PVA/Si). With sequential double sweeps of C-V measurements, hysteresis behaviors by flatband voltage (V_{FB}) shift could be detected. The C-V curve clearly shows the largest hysteresis (Fig. 4c) in the full device intervening with Au NPs.

In Fig. 4(a), it can be derived that the clockwise hysteresis (positive flatband voltage shift: $+\Delta V_{FB}$) is correlated with effect of mobile ions, carrier injection [15] and interface bound charges [16]. One of reasonable origins of C-V hysteresis is electron injection into the PVA layer. The positive shift at the negative gate voltage implies that electrons are transported from the top electrode to the PVA layer. Electron injection from the top electrode and trapping in the PVA layer is responsible for the hysteresis behavior under negative gate bias as was observed in Fig. 4(a). The other reason of C-V hysteresis is effect of mobile ions. The cross-linked PVA layer has some ions, such as the Cr^{2-} (negative mobile ions) from ammonium dichromate for the cross-linking step [13]. When the sample is applied negative bias, the ions are forced to move near silicon substrate, so the V_{FB} is shifted to right. In contrast, when the device is applied positive bias, the ions move to near gate. The charges locating near gate contribute to cause no V_{FB} shift [16,17], so the V_{FB} should be nearly the same as the case with no charge within insulator. In other words, the forward sweep line is getting positively shifted while the backward sweep line has no changes in Fig. 4(a) and it shows the clockwise hysteresis [17].

In Fig. 4(b), it shows that clockwise hysteresis ($+\Delta V_{FB}$) from metal/pentacene/APTES-coated PVA/Si is bigger than metal/PVA/Si case in Fig. 4(a). It is correlated with effect of mobile ions and top electrons injection. Electrons from the top electrode can be injected into the pentacene layer, giving rise to a positive shift [17,18]. The clockwise hysteresis ($+\Delta V_{FB}$) is thus correlated with the electron injection from the top electrode. Therefore, electron injection from the top electrode and trapping in the pentacene layer is responsible for the hysteresis behavior under negative gate bias observed in Fig. 4(b).

Fig. 4(c) shows the positive shift at the negative gate voltage implies that electrons are transported from the top electrode to the Au NPs. These electrons are discharged during sweep from the positive voltage. In Fig. 4(c), when the gate sweep voltage is increased from $(-/+)$ 5 V to $(-/+)$ 7 V, the forward sweep line is positively shifted and the backward sweep line is negatively shifted, respectively. It demonstrates that the Au NP charging shows a positive V_{FB} shift (forward sweep line) by electron injection from gate electrode to the Au NPs at the negative gate voltage. The full device also shows a negative V_{FB} shift (backward sweep line) by hole injection from top electrode to Au NPs at the positive gate voltage. In the process of sweep from the positive to negative voltage, injected electrons are discharged. At that time a slight strong positive gate voltage can inject hole from gate electrode to Au NPs.

The ΔV_{FB} of the full device (metal/pentacene/Au NPs/APTES-coated PVA/Si) was measured as 5.4 V for $(-/+)$ 5 V of sweep voltage and 8.6 V for $(-/+)$ 7 V. The ΔV_{FB} of control device without Au NPs (metal/pentacene/APTES-coated PVA/Si) was 3.1 V for $(-/+)$ 5 V of sweep voltage and 3.9 V for $(-/+)$ 7 V. Therefore, we can assume that the charge density of Au NPs is about $1.73 \times 10^{12} \text{ cm}^{-2}$ at the $(-/+)$ 7 V and $8.48 \times 10^{11} \text{ cm}^{-2}$ at the $(-/+)$ 5 V programming condition. These values can be calculated with a pentacene dielectric constant and a thickness of 60 nm by the following Eq. (1).

$$\Delta V_{FB}(\text{full_device} - \text{control_device_without_Au_NPs}) = -\frac{1}{\epsilon_{\text{pentacene}} \times \epsilon_0} (Q_{\text{pentacene}} \times t_{\text{pentacene}}) \quad (1)$$

where $\epsilon_{\text{pentacene}}$ is the dielectric constant of pentacene and ϵ_0 is the permittivity of free space, $Q_{\text{pentacene}}$ are the charge density at the pentacene layer of the Au NPs, respectively, while $t_{\text{pentacene}}$ (thickness of pentacene) is the distance between top electrode and Au NPs layer.

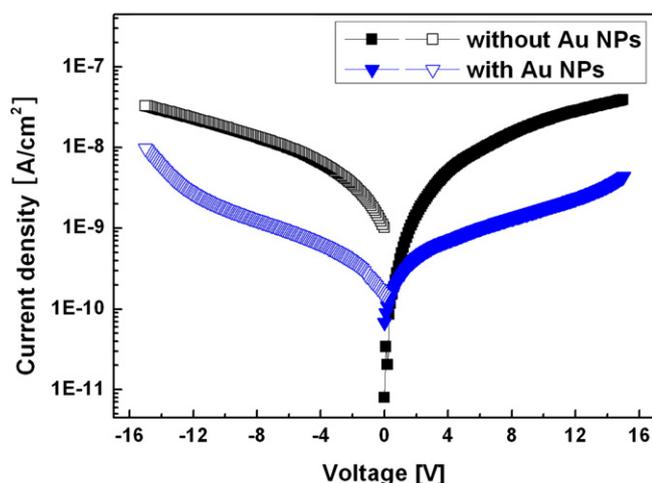


Fig. 5. Current-voltage (*I*-*V*) relations of MPIS structures with/without Au NPs.

The charges in both Au NPs and trap sites can be utilized to obtain the memory characteristics. However, the charges stored in the traps with different energy levels may cause the deviation of the retention characteristic, which eventually limits the application to highly integrated devices [18,19]. To clarify the effect of charges at trap sites, the study on the trap density, location, and their energy levels is further required.

Fig. 5 shows the current-voltage (*I*-*V*) relations of the MPIS structure with or without Au NPs. In Fig. 5, current was measured by scanning the gate voltage from zero to positive or negative bias. A low leakage current was found for both capacitors, which reveals the highly insulating characteristic of the pentacene/PVA films. However, the leakage current of the full device containing Au NPs is more significantly suppressed, as compared with that of the control device without Au NPs [4]. The decrease in leakage current results from two reasons: (1) as the carriers inject into the Au NPs, the Coulomb blockade effect prevents further injection and storage of more carriers and (2) the compensation of the external electrical field by the internal electrical field built up by the charges stored in the Au NPs during measurement [4,20]. However, additional investigations are required for elucidating the major reason.

4. Conclusion

In summary, metal-pentacene-insulator-semiconductor memory structures have been fabricated incorporating Au NPs as the charge

storage elements. Using C-*V* measurements, the device was shown to exhibit memory characteristics, with a memory window depending on the sweep voltage. Relatively wide memory windows with square-shaped hysteresis curves could be achieved for Al/pentacene/Au NPs/APTES-coated PVA/Si structures. The main driving force of C-*V* hysteresis is charging electrons and holes in both Au NPs and trap sites. In have a robust device characteristic, the effect of charges at trap sites should be more controlled.

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