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Nonvolatile floating gate organic memory device based on pentacene/CdSe quantum dot heterojuction

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An organic floating-gate memory device using CdSe quantum dots (QDs) as a charge-trapping element was fabricated. CdSe QDs were localized beneath a pentacene without any tunneling insulator, and the QD layer played a role as hole-trapping sites. The band bending formed at the junction between pentacene and QD layers inhibited back-injection of holes trapped in CdSe into pentacene, which appeared as a hysteretic capacitance-voltage response during the operation of the device. Nearly, 60% of trapped charge was sustained even after 10^4 s in programmed state, and this long retention time can be potentially useful in practical applications of non-volatile memory.
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Semiconductor nanocrystals (NCs) have been intensively investigated because of their potential applications in electronic and optoelectronic devices, such as light-emitting diodes,[1] field-effect transistors,[2] and solar cells.[3] In particular, nonvolatile memory devices fabricated with NCs have emerged as a promising candidate for the development of next-generation memory device.[4–6] The utilization of NCs in floating gate offers several important advantages. First, NCs permit the use of a thinner tunneling oxide layer, which can lead to long term charge retention (at least 10−20 years).[7,8] In addition, the thinner oxide layer can lower program/erase voltage, which results in less damage, larger endurance for write/erase cycles, and improved reliability. Second, band structure engineering methods, such as tuning band-offsets and barriers, are possible through a combination of various NCs.[9–11] The memory devices based on NCs, therefore, provide several merits including low power consumption, small device size, excellent stress-induced leakage current immunity, and better retention originated from the structural traits.

Herein, we report a NC-based organic memory device that utilized CdSe quantum dots (QDs) as a charge-trapping element. A unique feature of our device is that unlike the traditional pentacene-based device configuration, it has no tunneling insulator inside. Instead, a thin layer of QDs directly contacts with a pentacene layer, creating a type II junction. Interestingly, we observed a great hysteretic behavior in our device and also found that nearly 60% of charge carriers trapped in the QDs could be sustained even after 10^4 s in programmed state.

Tunneling insulator is one of the vital components in memory devices, which can strongly affect their performance. It prevents the escape of trapped charge carriers from floating gate. In general, floating gate memory devices have employed organic or inorganic insulators with high resistivity and thermal stability to ensure reliable charge retention. A polymer such as polymethylmethacrylate (PMMA) has been utilized as an insulator, showing good electrical properties with little hysteresis in capacitance-voltage (C-V) and current-voltage (I-V) curves.[12] With the large energy gap between highest-occupied molecular orbital (HOMO) and lowest-unoccupied molecular orbital (LUMO), the polymer tunneling insulator can inhibit the back-injection of captured charge to pentacene layer, permitting programmed state to be retained in the memory device.

The most ideal characteristics of a tunneling insulator is that it should inhibit the dissipation of the restored charge without increasing the resistivity of a device upon initial charge injection. To date, however, there is no such tunneling insulator developed. On the other hand, in the absence of a tunneling insulator, the charge injection can occur directly from pentecene to charge trapping sites. Since there is no resistive dielectric, it is expected that charge carrier trapping can be readily achieved with a lower threshold voltage, but the charge trapping cannot be long-lasting. Interestingly, if pentacene and the charge trapping sites were put together such that they can create an interface with a type II band alignment, the charge trapping can be significantly prolonged because of band bending formed at the junction. In this study, we paid attention to the energetic characteristics of pentacene and 5 nm-sized CdSe QDs for this approach. Pentacene, a semiconductor, possesses 2.0 eV of energy gap with its HOMO (–5.0 eV) and LUMO (–3.0 eV) level, whereas CdSe QD (5 nm in diameter), a charge trapping site, has 3.5 eV of band offset with its conduction and valence band positioned at –3.55 and –6.55 eV, respectively. This implies that an extra energy barrier due to the type II band bending exists at the heterojunction between pentacene and CdSe QD layers when the two layers are directly assembled.[13] Therefore, when the charge carriers are trapped, the charge trapping can last long enough for the operation of memory device quite a long time. Consequently, in this configuration, a dielectric insulator layer

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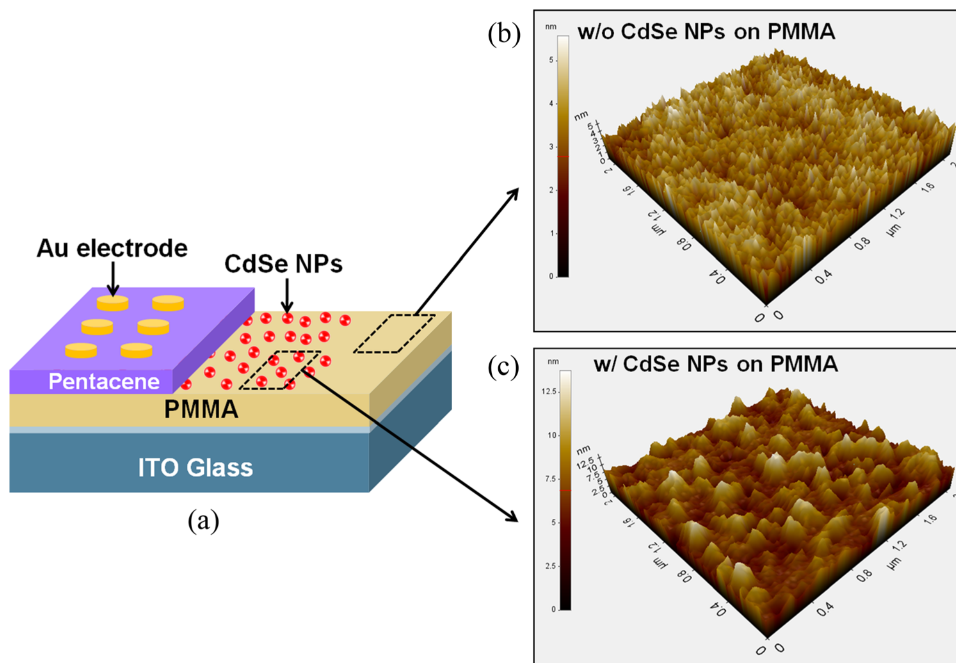

FIG. 1. (a) Schematic diagram of the device architecture with a bottom-gate organic nonvolatile memory device; Atomic force microscope (AFM) image of devices without CdSe QDs (b) and with CdSe QDs (c) on PMMA gate insulator.

between semiconductor and charge trapping sites, which has been an indispensable part of memory device, is no longer required for memory device.

Figure 1(a) is a schematic illustration of an organic memory device comprised of a layer of CdSe QDs beneath a pentacene layer. CdSe QDs were prepared by hot injection method with some modifications.[14] The metal-insulator-semiconductor structure was built on indium tin oxide (ITO), a bottom-gate electrode. PMMA (molecular weight of 950 K, diluted in 4% anisole) gate insulator and CdSe QDs (5 nm in diameter, 10^{16} particles/ml in toluene) were spin-coated on the ITO surface, and the device was then baked in a conventional oven. An atomic force microscope observed the topology of PMMA surface before and after the deposition of CdSe layer, revealing that the CdSe QDs were clustered in hundreds of nanometers, and the agglomerated CdSe QDs were fairly evenly distributed over the PMMA surface (Figs. 1(b) and 1(c)). A pentacene layer (~70 nm in thickness) following Au top electrode (~500 μm in diameter) was directly deposited on the CdSe QD layer using thermal evaporation.

Figure 2(a) shows the capacitance-voltage (C-V) behavior of memory devices fabricated with CdSe QDs, denoted as <ITO|PMMA|CdSe QDs|pentacene|Au>, measured at 100 kHz. Three kinds of cyclic bias voltage (V_{bottom}) was applied from positive to negative direction on the bottlm electrode (i.e., ITO electrode) with increasing the sweep range from ±10 V to ±30 V. While a control device fabricated without CdSe QDs shows no hysteresis (Fig. 2(b)), the device with the CdSe QD layer clearly displays hysteresis loops in a counterclockwise direction upon sweeping the V_{bottom} in various sweep range. This behavior indicates that a significant number of charge-trapping sites exist inside the CdSe QD layer (and/or its interface) whereas negligible in the absence of the QDs. Our claim was also supported by monitoring the change in flat-band voltage (V_{FB}) during voltage sweep. The V_{FB} can be obtained when an applied V_{bottom} equals to the workfunction difference between the bottom metal electrode and the semiconductor. If there is a variation in charge density in the insulator and/or at the insulator-semoconductor interface, V_{FB} should vary accordingly to reflect the change in energy level. The gradual negative shift in V_{FB} was indeed observed upon increasing the sweep range from ±10 V to ±30 V, which indicates holes were injected into the CdSe QD layer from the pentacene layer directly. The hysteresis loop in the C-V curve, representing memory window, became wider as the voltage sweep range increased because of increased charge injection. It should be noted that almost no shift was observed at various sweep ranges when the V_{bottom} was swept from positive to negative direction. This observation suggests that it is more efficient to charge the CdSe QDs positively than negatively in our device. The energy band diagram of our device is described in Fig. 2(c). Energetically, the coupling of pentacene and CdSe QD layers can form type II band alignment, which results in band bending at the heterojunction.[13] When a sufficiently large electric field is applied (negative V_{bottom}), holes can tunnel into the valence band of the CdSe QDs from the HOMO level of the nearby pentacene molecules. The extra energy barrier created by the type II band alignment accounts for significantly prolonged hole trapping in CdSe QDs even after the negative V_{bottom} is removed.

Figure 3 shows a typical program/erase operation for the fabricated devices. The "programmed" state refers to the transfer of holes from the pentacene to the CdSe QDs while applying a negative bias to the bottom electrode. The reverse operation is defined as the "erased" state, in which the charges stored in the CdSe QDs move back to the pentacene layer after a positive bias voltage is applied. The programmed and erased states were monitored by observing the shift in C-V curve as a function of the amplitude of applied positive or negative V_{bottom}. After program/erase operation, V_{bottom} was swept from +10 to –10 V with the memory window (ΔV) measured at a capacitance of 18.89 pF. In order to

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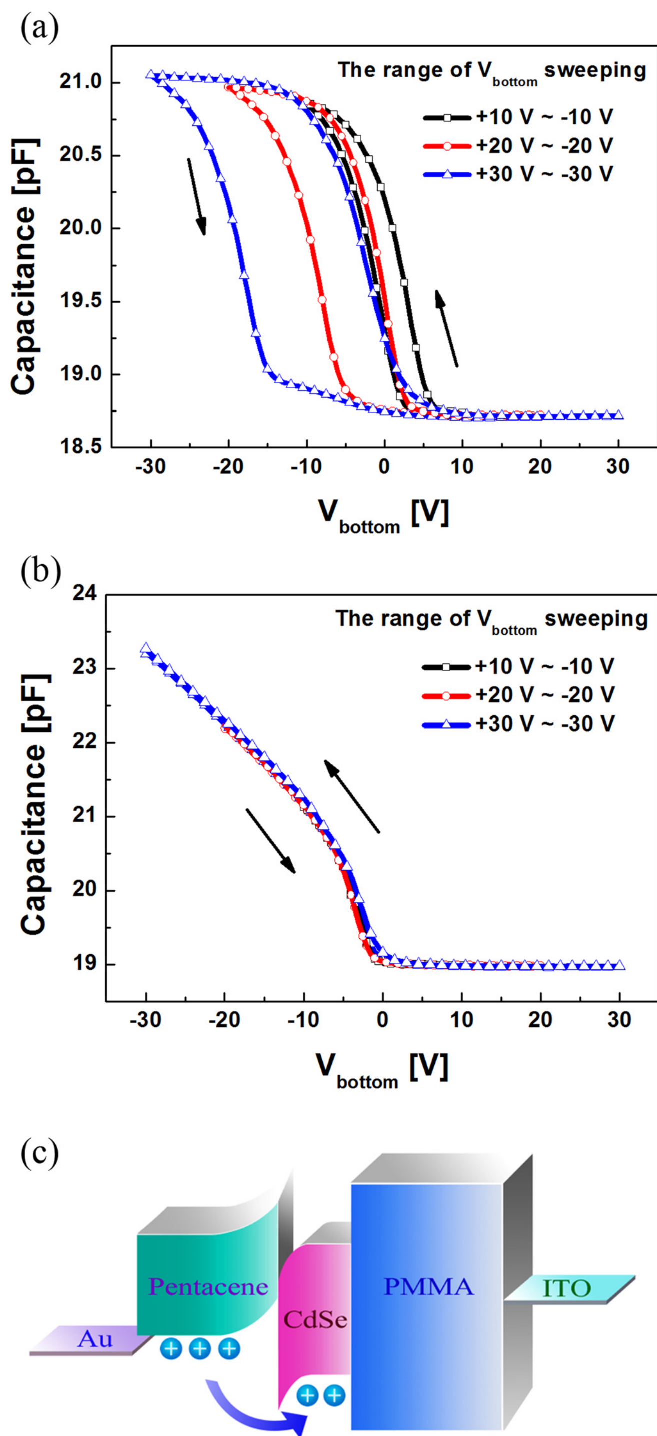

FIG. 2. C-V characteristics of the fabricated organic memory at different V_{bottom} sweeping range (a) with CdSe QDs, (b) without CdSe QDs and (b) energy band diagram of memory device.

exclude the influence of read disturbance (the voltage sweep), continuous voltage sweep from +10 to –10 V without program/erase operation was conducted (only 1st and 2nd measurements are given in Fig. 3). After the initial voltage sweep (the 1st measurement), the C-V curve shifted to negative direction in the 2nd measurement due to the positive charging of CdSe QDs upon V_{bottom} sweping from +10 to –10 V. From the 2nd measurement and repeated measurements under the same condition, the signal remained fairly stable and almost no shift in C-V curve was observed (data not given for repeated measurement), ensuring that no read

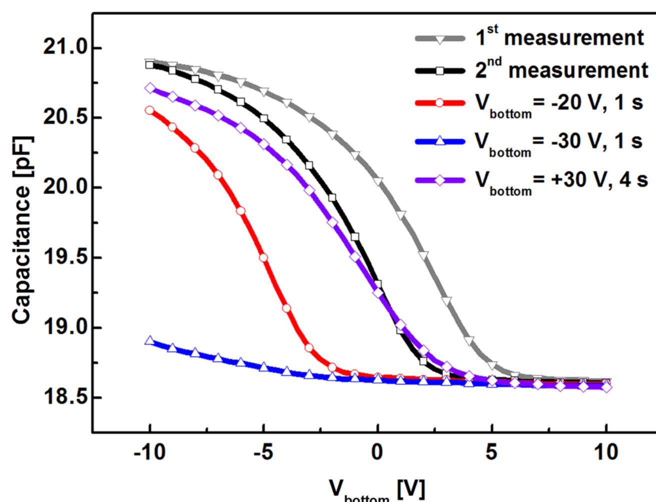

FIG. 3. Capacitance change (ΔC) as a function of bottom electrode stress voltage.

disturbance was included in our analysis. C-V curve shifted to negative direction when V_{bottom} of –20 and –30 V were applied for 1 s. On the other hand, it slightly shifted towards positive direction after erasing the memory by applying V_{bottom} of +30 V for 4 s. The ΔV was approximately –4.59 and –11.29 at V_{bottom} of –20 and –30 V, respectively. The negative ΔV is attributed to the positive charging of CdSe QDs upon applying negative V_{bottom}. The charge density of the CdSe QDs can be estimated from $Q = C\Delta V$, where C is the capacitance between the gate and the CdSe QDs.[15] CdSe QDs was estimated to possess the positive charge density of 3.51×10^{11} and 8.63×10^{11} ea/cm^2 for V_{bottom} of –20 and –30 V, respectively.

The charge retention characteristics of the fabricated device were determined from the time-dependent change in capacitance after programming (Fig. 4). After programming at V_{bottom} of –30 V for 1 s, V_{bottom} was swept from 2 to –2 V with ΔC measured at a V_{bottom} of 0 V during a sweep in order to minimize read disturbance. The device with CdSe QDs possessed a capacitance of 18.67 pF at 0 V just after being programmed. Interstingly, almost ∼60% of trapped charge

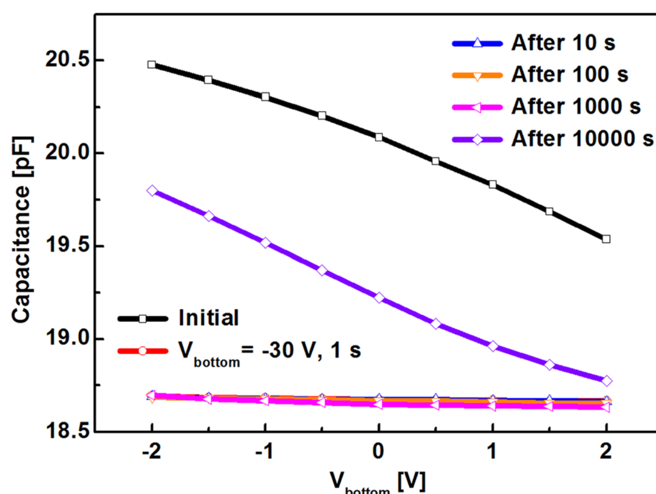

FIG. 4. Retention characteristics after applying −30 V gate stress voltage for 1 s.

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was sustained even after 10^4 s in programmed state, showing 19.22 pF at 0 V. This observation supports our claim that the holes are efficiently trapped and confined in CdSe QDs becuase of the existance of extra energy barrier near the heterojunction. This long retention time of our device can be potentially useful in practical applications of non-volatile memory devices. We are currently investigating the characteristics of our device upon controlling several critical parameters such as QD sizes and insulator thickness to further optimize its performance.

In summary, we demonstrated the fabrication of a non-volatile organic memory device without using a tunneling insulator layer. Our device utilized a heterojunction created by coupling petancene and CdSe QD layers. The type II band alignment formed at the pentacene/CdSe QDs heterojunction induces energy barrier near the heterojunction interface. The charging and discharging behavior of CdSe QDs was observed in the C-V analysis of MIS structure, showing that the sufficiently large memory window and good retention characteristics can be achieve with our configuration. We believe that this approach, by virtue of its simplicity in processing, can open up a opportunity towards the development of next-generation organic memory device.

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