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Organic memory device with polyaniline nanoparticles embedded as charging elements

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Polyaniline nanoparticles (PANI NPs) were synthesized and fabricated as charging elements for organic memory devices. The PANI NPs charging layer was self-assembled by epoxy-amine bonds between 3-glycidylpropyl trimethoxysilane functionalized dielectrics and PANI NPs. A memory window of 5.8 V (ΔV_{FB}) represented by capacitance-voltage hysteresis was obtained for metal-pentacene-insulator-silicon capacitor. In addition, program/erase operations controlled by gate bias ($-/+90$ V) were demonstrated in the PANI NPs embedded pentacene thin film transistor device with polyvinylalcohol dielectric on flexible polyimide substrate. These results can be extended to development of fully organic-based electronic device. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4704571]

Recently, high performance organic memory devices have been developed for large area flexible electronics, low-cost dispensable sensor arrays, and memory tags.[1–5] Particularly, a number of active researches have been focused on organic devices using nanoparticles (NPs).[1–3] So far, metal NPs for charging elements of memory device have been intensively demonstrated with development of self assembly monolayer (SAM) method.[2–4] For NPs embedding in organic memory device, 5–20 nm sized NPs could be allowed high density to form nano floating gate with discrete charge storage. For example, gold (Au) NPs could be deposited in monolayer by Langmuir-Blodgett method or biological binding mechanism.[2,3] In addition, silver (Ag) NPs could be adopted to fabricate memory thin film transistors (TFTs) and even the memory TFTs could be realized on flexible substrate with high reliability.[4,5]

Polyaniline (PANI) is one of thoroughly studied conducting polymers and often reported to be synthesized in emulsion polymerization process accompanying micelle forming and doping.[6–8] The PANI can be synthesized in NPs form with environmental stability, doping capabilities through the introduction of acid or base, and unique alignment of crystallinity. Specially, with dodecylbenzenesulfonic acid (DBSA), synthesis of PANI NPs dispersed in aqueous phase has been widely reported.[6–8] The surfactant or doping agent could result in conductance difference by the orders of magnitude in the PANI NPs synthesis.[7] The PANI NPs has been reported that as the size of the NPs decreases, the conductivity increases due to an increase of degree of doping and crystallinity. The simple polymerization method could produce 10 ± 2 nm diameter PANI NPs, of which emeraldine form is a completely deprotonated form of polymer.[7,8] However, the applications of the PANI NPs to organic electronics have been limited to form source/drain electrodes.[9,10] Moreover, further applications of the PANI NPs other than elec-

trodes of organic electronics have been retarded due to poor processability.[7,8]

Amine ($-NH_2$) group in organic molecule was reported to have a mild physical adsorption subsequently having a fast intramolecular covalent binding with epoxy group.[11] Since the epoxy groups are very stable at neutral pH even in aqueous condition, the epoxy-activated surface seems to be ideal for anchoring or immobilization of amine containing organic NPs.[11] Furthermore, epoxy functional groups are able to react with different nucleophile group, such as hydroxyl ($-OH$) and thiol ($-SH$). Since the PANI NPs has amine groups in its nano-sized molecules, the covalent bond, or epoxy-amine bond between the epoxy-functionalized surface and the PANI NPs, can be realized. Recently, chemical reagent of 3-glycidylpropyl trimethoxysilane (GPTMS) was reported to have a strong covalent epoxy-amine bond with amine group of a chemical reagent, 3-aminopropyl triethoxysilane (APTES). In addition, the covalent bonding was efficiently enhanced by substrate heating at 80 °C.[12]

In this study, PANI NPs were synthesized with DBSA and the PANI NPs were used as charging elements in capacitor memory device of meal-pentacene-insulator-silicon (MPIS) device and pentacene TFTs device on flexible substrate of polyimide (PI). The PANI NPs were self assembly monolayered on dielectric layer by epoxy-amine bond strategy realized by anchoring amine-terminated PANI NPs and epoxy-terminated GPTMS surface.

A simplified polymerization procedure for the synthesis of PANI NPs was adopted.[7] Equimolar concentrations of DBSA and aniline were added with mechanical stirring in quartz reactor having a thermostated bath at 65 °C for 1.5 h. More detailed synthesis method is described in previous report.[6,7] The synthesized dark green dispersion of emeraldine PANI NPs was purified by dialyzing against ultrapure deionized (DI) water using dialysis membrane. After dialysis, the dispersion was centrifuged to obtain the supernatant containing nano-sized PANI.

For fabrication of MPIS memory capacitor device, 10 nm thick thermal grown SiO_2 is formed on p-type boron

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doped (100) silicon wafer having a resistivity of 10-15 Ω-cm. The SiO_2 surface was first functionalized with GPTMS by immersing the substrate in 5% vol. GPTMS in ethanol for 1 h. The PANI NPs were assembled on epoxy-terminated SiO_2 by immersing the substrates into the PANI NPs solution in ethanol for 12 h at *p*H 6. After formation of the PANI NPs monolayer, the substrate was annealed at 80 °C and sonicated with DI water to remove non-covalently bound PANI NPs.[12] Pentacene (60 nm thick) and top gold electrode (100 nm thick and 1.0 mm radius size) are then deposited via sequential thermal evaporation. For the fabrication of pentacene TFTs memory device, flexible PI substrate and 200 nm polyvinylalcohol (PVA) dielectric layer were used. The PVA layer was prepared as previously reported.[13] High resolution transmission electron microscopy (HRTEM) images were taken by Philips XL30SFEG microscopy. The selected area electron diffraction (SAED) was obtained by JEOL JEM 2100 F microscopy at an accelerating voltage of 200 keV. High resolution scanning electron microscopy (HRSEM) image for the monolayered PANI NPs was obtained with Field Emission Scanning Electron Microscopy (FESEM) (JEOL JSM 7000 F). Surface charges of the PANI NPs were measured in the form of zeta potentials by an electrophoretic light scattering spectrophotometer (ELS 8000, Otsuka). Capacitance-voltage (C-V) measurements were performed by Agilent 4284 A at the frequency of 100 kHz and 1 MHz. The performance of pentacene memory TFTs were measured by Agilent 4145B with programmable gate bias of −90 V and erase bias of +90 V.

Figure 1 shows (a) HRTEM image and SAED image of synthesized PANI NPs, (b) schematic diagram for PANI NPs self assembly formation on GPTMS functionalized dielectrics, and (c) HRSEM image of monolayered PANI NPs. Inset of Fig. 1(a) shows SAED pattern of PANI NPs with well-defined diffraction spots. The SAED patterns corresponded to (011), (110), (002), and (112) with d-spacings of 0.2639, 0.2159, 0.1583, and 0.1284 nm, respectively,[7] which proves that the synthesized PANI is semicrystalline polymer. Fig. 1(b) shows a schematic chemical reaction scheme to have monolayered PANI NPs on epoxy functionalized surface. By introduction of the covalent bond scheme in Fig. 1(b), the monolayered PANI NPs image was obtained in Fig. 1(c). In order to reduce non-chemical bonding between PANI NPs and GPTMS functionalized SiO_2 or PVA dielectric layers, the PANI NPs were suspended into ethanol instead of DI water. Table I shows surface zeta potentials of the PANI NPs in DI water and ethanol. It shows that the surface zeta potentials in DI water and ethanol were measured as −39.01 mV and +25.78 mV, respectively. The difference of absolute value (39.01 mV to 25.78 mV) of the surface zeta potentials indicates that the covalent epoxy-amine bond between the PANI NPs and GPTMS surface rather than undesirable electrostatic binding would be favored in ethanol solvent.[3] Fig. 1(c) shows that no severe agglomeration of the PANI NPs was detected. The agglomerated particles could be a source of defects in memory devices. Based on the Fig. 1(c) SEM image, a spatial density of individual PANI NPs could be counted in average as $1.82 \times 10^{10}/cm^2$.[3,14]

Figure 2 shows (a) C-V result showing counter-clockwise hysteresis and (b) electrical retention test obtained
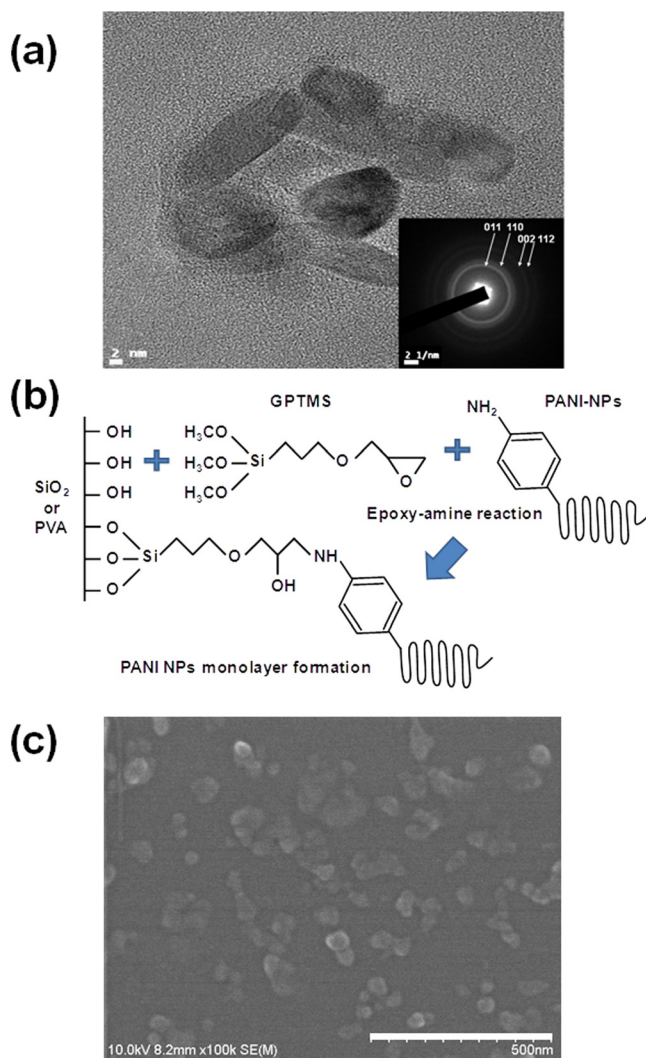

FIG. 1. (a) HRTEM and SAED image of synthesized PANI NPs, (b) schematic diagram for self assembly formation of PANI NPs on GPTMS functionalized dielectrics, and (c) HRSEM image of the monolayered PANI NPs.

from capacitor device. The voltage was referenced from the top electrode in the MPIS structure. In Fig. 2(a), a C-V hysteresis window of 5.8 V in the full device was detected with sweep range of (+/−) 7 V. However, declined slope of C-V at accumulation region was observed, which can be an index of degradation of organic layers.

The ΔV_{FB} can be approximately estimated by an equation given in previous report.[3] The ΔV_{FB} is equal to Q_{NPs}/C_{MPIS} where Q_{NPs} is the total charges trapped in the NPs and C_{MPIS} is the capacitance of the reference MPIS device. As shown in Fig. 2(a), with the ΔV_{FB} of 5.8 V of (+/−) 7 V sweep, the total charges trapped in NPs is calculated with C_{MPIS} (=280 pF) is 4.81×10^{-11} C. It corresponds to a spatial charge density of $1.21 \times 10^{11}/cm^2$ if one charge is presumed to occupy one PANI NP. Since the spatial charge density counted from the FESEM was $1.82 \times 10^{10}/cm^2$ in

TABLE I. Zeta potentials of PANI NPs in DI water and ethanol.

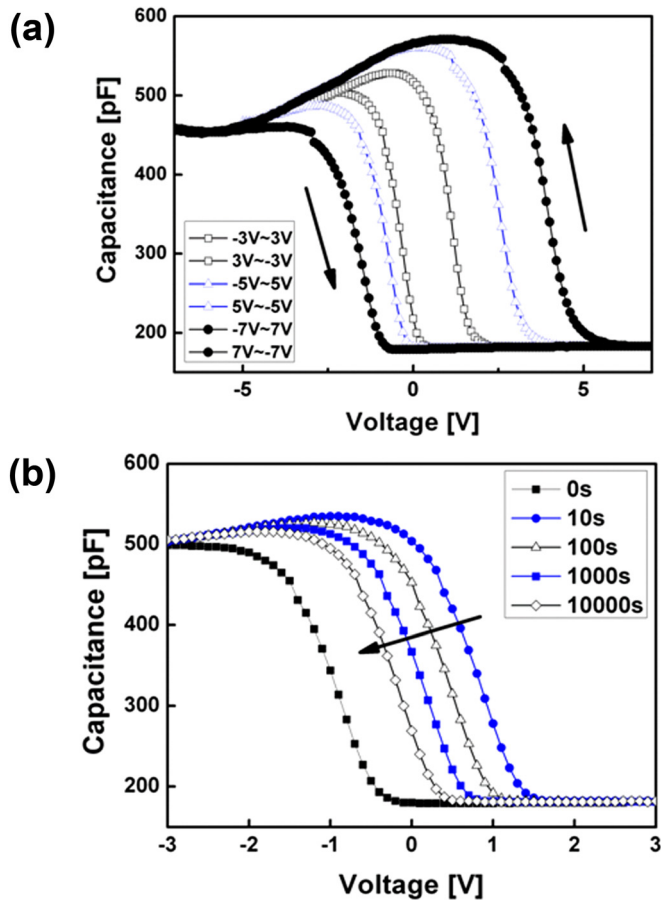| Solvent	In DI water	In ethanol
Zeta potential (mV)	−39.01	+25.78

(a)

(b)

FIG. 2. (a) Counter-clockwise C-V characteristics and (b) electrical retention test of memory device having 10 nm SiO_2 PANI NPs embedded MPIS device.

(a)

(b)

(c)

FIG. 3. (a) Topography image, (b) EFM image on pentacene layer with PANI NPs on GPTMS functionalized SiO_2 (10 nm) with +6 V bias at p-Si side, and (c) EFM image with −6 V bias at p-Si side.

Fig. 1(c), the charge storage effect by one PANI NP should be higher than 6 charges. This phenomena is believed to be originated from large size (10 ∼ 50 μm) of PANI NPs monolayered on SiO_2 surface compared with 5 ∼ 10 nm sized Au or Si NPs, which were typically adopted as charging elements.[3,5,13,14] The retention could be kept for 10 000 s as shown in Fig. 2(b), which was comparable to MPIS device with metal or inorganic NPs.[14]

Figure 3 shows (a) topography image, (b) electrostatic force microscopy (EFM) image on pentacene layer with PANI NPs on GPTMS functionalized SiO_2(10 nm) with +6 V bias at p-Si side, and (c) EFM image with −6 V bias at p-Si side. The topological existence of PANI NPs under pentacene layer was detected as shown in the topography of Fig. 3(a). As shown in Figs. 3(b) and 3(c), the EFM image demonstrated that the PANI NPs were electro-statically charged. The locations of indentations and protrusions shown in Figs. 3(a)–3(c) were roughly matched, which indicated that the topology and the charging are dependent upon the existence of the PANI NPs monolayer. In addition, the electrostatic effect was more pronounced with −6 V bias as shown in Fig. 3(c) than +6 V bias in Fig. 3(b). It indicates that electron charging in the PANI NPs through very thin oxide layer was more effective than hole charging in the PANI NPs.[3] The result coincides with Fig. 2(a), which shows that wider hysteresis loop appears when the top electrode is positively biased or swept than negatively biased or swept.[13,14]
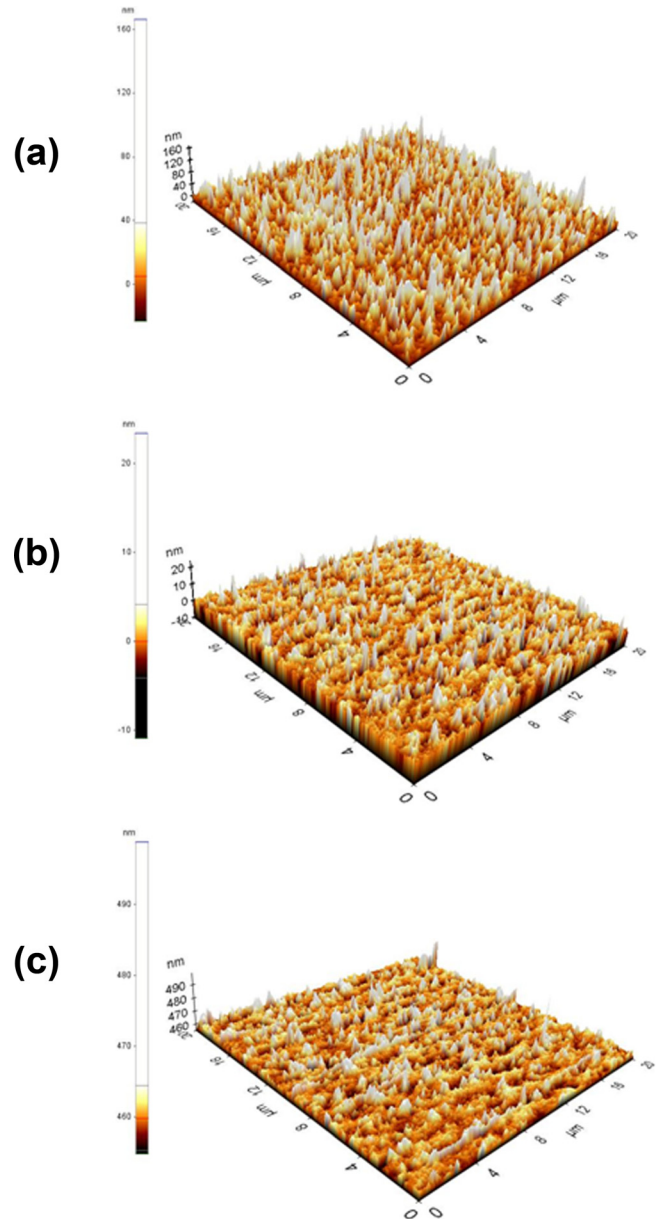
Figure 4 shows (a) microscopic image of pentacene memory device embedded with PANI NPs on flexible PI substrate, (b) output characteristics of PANI NPs embedded TFT (inlet: output characteristics of pentacene TFT having PVA dielectric without PANI NPs), and (c) transfer characteristics of PANI NPs embedded TFTs with −90 V program or re-program bias and +90 V erase bias. Inlet graph of Fig. 3(b) shows that output characteristics of pentacene TFTs without PANI NPs embedding shows a saturation current behavior. However, with PANI NPs embedding, the output characteristics show a depleted state output behavior, which does not show a saturation I_{DS} as shown in Fig. 4(b). In addition, in output characteristics of Fig. 4(b), it was shown that gate leakage currents under low source-drain voltage (V_{DS}) conditions for both non-memory TFTs and PANI NPs embedding memory TFTs.
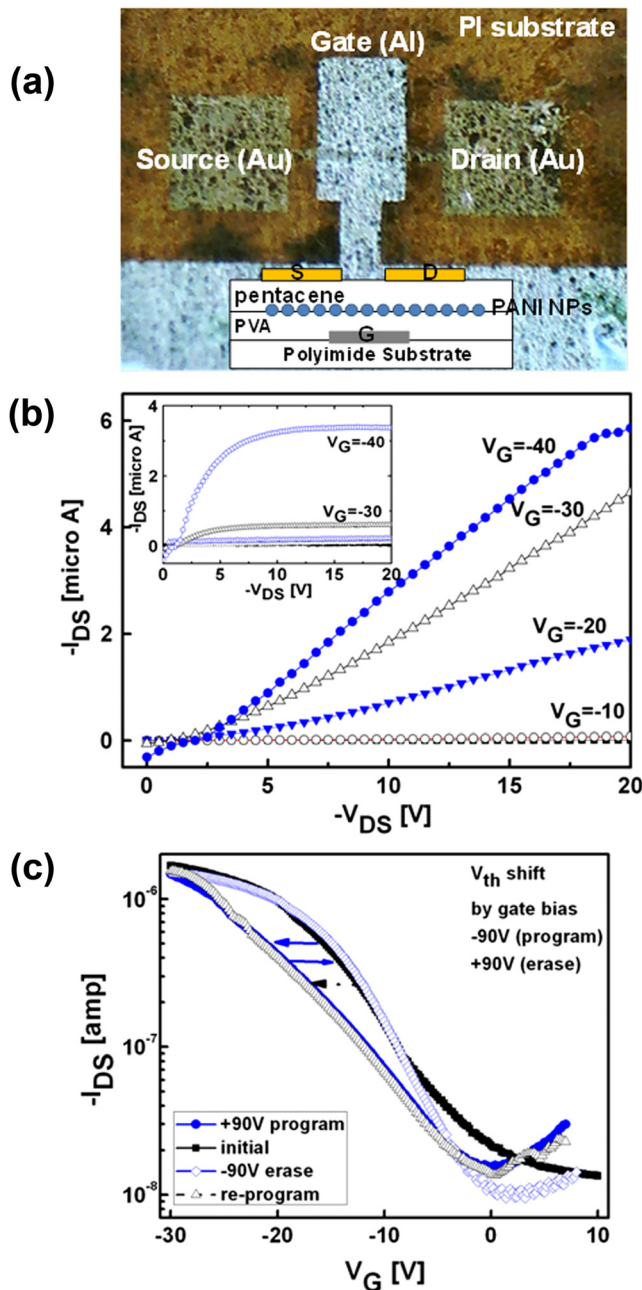
FIG. 4. (a) Microscopic image of pentacene memory device embedded with PANI NPs on flexible PI substrate, (b) output characteristics of PANI NPs embedded TFT (inlet: output characteristics of pentacene TFT having PVA dielectric without PANI NPs), and (c) transfer characteristics of PANI NPs embedded TFTs with −90 V program or re-program bias and +90 V erase bias.

In Fig. 4(c), threshold voltage (V_{th}) shifts with pentacene thin TFT devices were detected with the program/erase (−90 V/+90 V) biases. Program and re-program biases did not produce significant differences in output characteristics

as shown in Fig. 4(c). In this study, separate measurements with gate bias of (+/−) 45 V, apparent program-erase operations could not be obtained. The limited bias voltages attainable for program were also reported in previous literature, where the gate bias after 80 V was effective.[5] As shown in Fig. 4(c), initial V_{th} was −3.10 V and −9.42 V for programmed TFTs, respectively. The PANI NPs embedded TFTs exhibited a mobility of 0.15 cm^2/V·s with on/off ratio of $10^{2.2}$. No noticeable threshold voltage shift was detected on pentacene TFTs having PVA dielectric without PANI NPs embedding.[5,13] However, slightly leaky nature of PVA dielectric (as shown in Fig. 4(b)) and depleted TFT operational condition were believed to have short data retention capability of the PANI NPs for the charging effects.

In conclusion, organic PANI NPs was adopted as charging elements in nonvolatile memory devices in structures of MPIS and TFTs. This result can be contributed to a further step to realize an entirely organic or plastic electronics for memory device application.

[1]W. L. Leong, P. S. Lee, S. G. Mhaisalkar, T. P. Chen, and A. Dodabalapur, Appl. Phys. Lett. **90**, 042906 (2007).

[2]M. F. Mabrook, C. Pearson, D. Kolb, D. A. Zeze, and M. C. Petty, Org. Electron. **9**, 816 (2008).

[3]S. M. Jung, H.-J. Kim, B.-J. Kim, T.-S. Yoon, Y.-S. Kim, and H. H. Lee, Appl. Phys. Lett. **97**, 153302 (2010).

[4]S. Wang, C.-W. Leung, and K. L. Chan, Org. Electron. **11**, 990 (2010).

[5]S.-J. Kim and J.-S. Lee, Nano Lett. **10**, 2884 (2010).

[6]C. Y. Yang, P. Smith, A. J. Heeger, Y. Cao, and J. E. Osterholm, Polymer **35**, 1142 (1994).

[7]M. G. Han, S. K. Cho, S. G. Oh, and S. S. Im, Synth. Met. **126**, 53 (2002).

[8]M.-C. Park, Q. Sun, and Y. Deng, Macromol. Rapid Commun. **28**, 1237 (2007).

[9]K. S. Lee, G. B. Blanchet, F. Gao, and Y.-L. Loo, Appl. Phys. Lett. **86**, 074102 (2005).

[10]J. E. Yoo, K. S. Lee, A. Garcia, J. Tarver, E. D. Gomez, K. Baldwin, Y. Sun, H. Meng, T.-Q. Nguyen, and Y.-L. Loo, Proc. Natl. Acad. Sci. U.S.A. **107**, 5712 (2010).

[11]C. Mateo, R. Torres, G. Fernandez-Lorente, C. Ortiz, M. Fuentes, A. Hidalgo, F. Lopez-Gallego, O. Abian, J. M. Palomo, L. Betancor, B. C. C. Pessela, J. M. Guisan, and R. Fernadez-Lafuente, Biomacromolecules **4**, 772 (2003).

[12]M. J. Lee, N. Y. Lee, J. R. Lim, J. B. Kim, M. Kim, H. K. Baik, and Y. S. Kim, Adv. Mater. **18**, 3115 (2006).

[13]B.-J. Kim, H.-J. Kim, S.-M. Jung, Y.-H. Kim, S. Ha, T.-S. Yoon, and H.H. Lee, Thin Solid Film **519**, 4319 (2011).

[14]Y.-H. Kim, S. M. Jung, T.-S. Yoon, Y.-S. Kim, and H. H. Lee, Electrochem. Solid-State Lett. **14**, H149 (2011).