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Nonvolatile organic memory devices with CdTe quantum dots

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ABSTRACT

The nonvolatile organic memory devices were fabricated utilizing CdTe quantum dots (QDs). QDs were used as a hole-trapping component in the memory device. We analyzed the electrical properties of the memory device fabricated with CdTe QDs by measuring the capacitance–voltage characteristics and retention time. A number of holes were trapped in CdTe from pentacene, which formed band bending between pentacene and QD layer. We observed large hysteresis at capacitance–voltage response during the operation of the device. The long retention of programmed state time of 10^4 s can be potentially useful in practical applications of non-volatile memory.

1. Introduction

Numerous studies have showed much interest on conventional nonvolatile memories over the last decade, due to their extensive usage in electronic equipment such as USB, computer DRAM memory chip, etc. However, organic non-volatile memory devices are also coming up with greater attention [1]. These organic memory devices are fabricated with organic semiconductors, but their electrical performances cannot catch up with those of inorganic memory device based on silicon. In most of the cases, memory devices which are necessary in complicated machines usually use inorganic semiconductors based on silicon. However, organic memory devices bear some advantages such as low temperature fabrication, cost effectiveness, and mechanical flexibility. Hence, organic electronics has become a popular field of study to many engineers [2–5]. Especially mechanical flexibility of organic electronics enables the manufacture of electronics that are different in shape. The reason why inorganic memory device is not flexible lies in the use of solid substrate. Fabricating organic electronic device in low temperature let plastic substrates endure the heat, which is impossible in the fabrication of inorganic memory device. These features can be used in high-technology industry fields such as wraparound computer, flexible display TV, etc.

Several types of gate dielectrics enable reversible trapping of charges upon application of a gate field, for instance polymer electrets [6], dielectrics with embedded metallic [7] or semiconducting nanoparticles (NPs) [8] with permanent and/or switchable electrical dipoles.

Among these technologies, organic memories based on NPs have attracted a great deal of interest because of their potential applications in next-generation memory devices. In general, metal NPs such as Au, Ag, and Cu have been utilized as charge-trapping elements for non-volatile memory devices [7,9,10]. In comparison to the metal NPs-based memory devices, the devices using semiconductor NPs as charge traps possess many intriguing properties and are therefore a powerful tool for the development and fabrication of materials with novel functions.

Among the various organic memory devices, semiconducting nanoparticles (NPs)-based organic memory is a promising candidate for the future nonvolatile memory [11,12]. In semiconducting nanoparticles-based organic memory, thin layer of NPs acts as a charge-trapping element by trapping holes from the pentacene layer [7–9]. Holes in the pentacene layer move to the layer of NPs due to the tunneling effect. As the holes enter the layer of NPs, nanoparticles capture the holes and change the *C–V* characteristics of the device. As various types of NPs exist, memory characteristics also can be controlled upon the structure and the type of NPs. A few significant studies were reported about NPs-based memory device with many interesting properties.

The utilization of NCs in floating gate offers several important advantages. First, NCs permit the use of a thinner tunneling oxide layer, which can lead to long term charge retention [7,8]. In addition, the thinner oxide layer can lower program/erase voltage, which results in less damage, larger endurance for write/erase cycles, and improved reliability. Second, band structure engineering methods, such as tuning band-offsets and barriers, are possible

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through a combination of various NCs [6,7,9]. Especially the electrical properties of memory device fabricated with CdSe NPs were studied recently. Kim et al., showed different kind of NPs, constructs different form of energy band which changes the electrical property of memory device [13]. However, the electrical properties of these memory devices according to the type of NPs have been still ambiguous.

Here, we present the performance variation of the organic memory device based on CdTe NPs. We analyzed the hole trapping effect by measuring *C–V* characteristics and retention time. Organic memory device used in this study is based on pentacene, an organic semiconductor. A unique feature of our device is that unlike the traditional pentacene-based device configuration, it has no tunneling insulator inside it. A thin layer of CdTe NPs were spin-coated as a single layer which directly connects the pentacene layer and PMMA layer, creating type II junctions [14].

2. Experimental

Fig. 1 shows a schematic illustration of an organic memory device comprising a layer of CdTe QDs beneath a pentacene layer and energy band structure of the organic memory with CdTe QDs. CdTe QDs were prepared by hot injection method with some modifications [15]. CdO (0.39 mmol), trioctylphosphine oxide (5.2 mmol), and tetradecylphosphonic acid (1.1 mmol) were degassed at 110 °C for 1 h and then heated under nitrogen to 315 °C so as to completely dissolve the precursors. TOPSe (0.25 mmol Se dissolved in 4.25 ml of trioctylphosphine) was subsequently injected into the hot solution to initiate the reaction. After the growth at 270 °C for 5 min, the NP solution was cooled until it reached to the room temperature. Finally it was washed three times with a mixture of methanol and toluene, and dissolved in toluene for use.

The metal–insulator–semiconductor (MIS) structure was fabricated on the indium tin oxide (ITO) glass substrate. The ITO layer was used in the size of 2×2 cm as a gate electrode. Substrates were cleaned by regular cleaning method: sonication with acetone, isopropanol, followed by rinsing in DI water and subsequently baking at 75 °C for 20 min. The gate insulator was polymethylmethacrylate (PMMA) with a molecular weight of 950 K diluted in anisole (5%). The PMMA layer was spin-coated and then baked at 160 °C for 30 min in a conventional oven, finally forming 200 nm thick PMMA layer. For making trap site, CdTe QDs were spin-coated on PMMA layer and subsequently baked at 100 °C for 10 min in a conventional oven. The approximate diameters of QDs were 5 nm, and the density of CdTe solution was 10 mg/ml. The pentacene layer was then deposited by thermal evaporation at a rate of 0.1–0.3 Å/s under high vacuum less than 5×10^{-6} torr. The final thickness of pentacene layer was 70 nm. Top metal electrode of gold was subsequently deposited by thermal evaporation through a shadow mask of 500 μm diameter size. These devices were characterized at room temperature in ambient air using a HP 4284A meter. The electrical properties of devices were analyzed by capacitance–voltage (*C–V*) characteristics at room temperature under ambient condition using HP 4284A LCR meter at a frequency of 100 kHz.

3. Results and discussion

To study the performance of organic floating-gate memory device using CdTe QDs which were localized beneath the pentacene, control devices were first studied. The control device fabricated without CdTe QD appeared no hysteresis when the bottom voltage (V_{bottom}) was swept from +10 to −10 V and then back to +10 V and even ±30 V (Fig. 2). No hysteresis indicates the absence of any charge trapping events inside PMMA and its interface. On the other hand, memory device containing CdTe NPs appeared hysteresis loops in counterclockwise direction while sweeping V_{bottom} at *C–V* curve. Fig. 3 shows the *C–V* curves of memory device containing CdTe QDs at a concentration of 10 mg/ml, measured at 100 kHz. Three kinds of cyclic V_{bottom} was applied from positive to negative direction on the bottom electrode (i.e., ITO electrode) with gradual increase the sweep range at ±10, ±20 and ±30 V (Fig. 3). The memory device with the CdTe QD layer clearly shows hysteresis loop in a counterclockwise direction upon sweeping the V_{bottom} in various sweep range. The inside of CdTe QD layer (and/or its interface) has lots of charge-trapping sites resulting in such loops. The change in flat-band voltage (V_{FB}) during voltage sweep also supports our claim. The V_{FB} can be obtained when an applied V_{bottom} equals to the work function difference between the bottom metal electrode and the semiconductor. V_{FB} should vary accordingly to reflect the change in energy level if there is a variation in charge density in the insulator and/or at the insulator–semiconductor interface. We observed gradual negative shift in V_{FB} with an increase of sweep range from ±10 to ±30 V. This means, holes were directly injected from the pentacene layer into the CdTe QD layer. The hysteresis loop in the *C–V* curve, representing memory window, became wider as the voltage sweep range increased due to increased charge injection. Interestingly, almost no shift was observed at various sweep ranges when the V_{bottom} was swept from positive to negative direction. This observation suggests that it is more efficient to charge the CdTe QDs positively than negatively in our device. The energy band diagram of our device is described in Fig. 1(b). Energetically, the coupling of pentacene and CdTe QD layers can form type II band alignment, because of band bending at the heterojunction. When large negative electric field is applied at bottom electrode, holes can move from the HOMO level of the nearby pentacene molecules to the valence band of the CdTe QDs.

Fig. 4(a) shows a typical program/erase operation for the memory devices. The "programmed" state means the movement of holes from the pentacene to the CdTe QDs while applying a

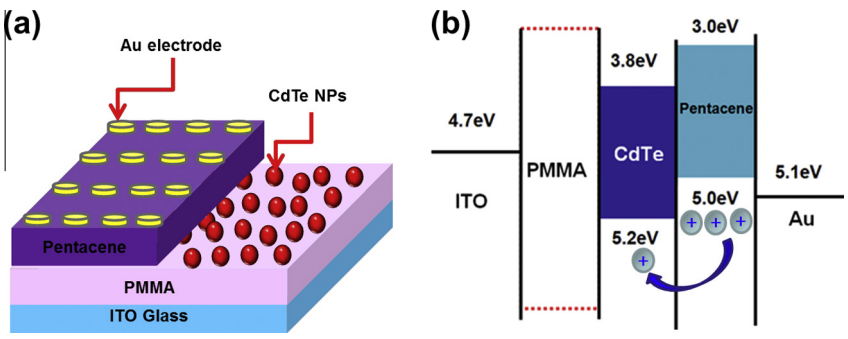

Fig. 1. (a) Schematic illustration of memory architectures and featuring CdTe QDs embedded in PMMA layer. (b) Energy band structure of the organic memory with CdTe QDs.

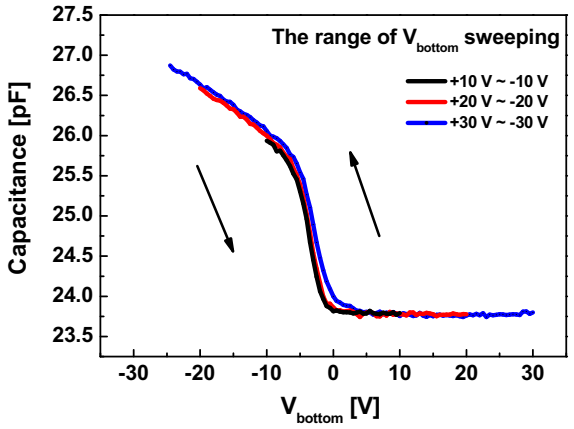

Fig. 2. *C–V* characteristic of the organic memory without CdTe NPs.

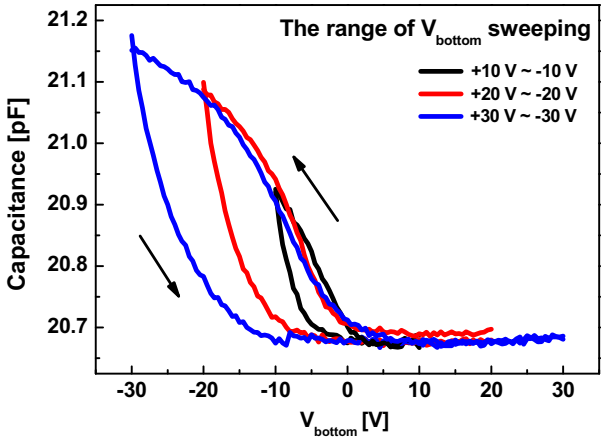

Fig. 3. *C–V* characteristic of organic memory with CdTe QDs at different V_{bottom} sweeping range.

negative electric field at the bottom electrode. The "erased" state refer to the stored charges (holes) in the CdTe QDs go back to the pentacene layer after a positive electric field applied to bottom electrode. The programmed and erased states were checked by observing the shift in *C–V* curve as a function of applied positive or negative V_{bottom}. In order to remove the effect of read disturbance (the voltage sweep), nonstop voltage sweep from +10 to −10 V without program/erase operation (1st and 2nd measurements are given in Fig. 4(a)). The *C–V* curve shifted to negative direction in the 2nd measurement owing to the positive charging of CdTe QDs upon 1st measurement (sweep from +10 to −10 V). After the 2nd measurement and continuous measurements below the equal condition, the signal remained equally constant and almost no shift in *C–V* curve was observed, confirming that no read disturbance was contained within analysis. *C–V* curve shifted to negative direction when V_{bottom} of −20 and −30 V were applied for 1 s. Moreover, a slight shift was observed towards positive direction after erasing the memory by applying V_{bottom} of +30 V for 3 s. The △V was approximately −1.62 and −5.19 at V_{bottom} of −20 and −30 V, respectively. The negative ΔV is attributed to the positive charging of CdTe QDs upon applying negative V_{bottom}.

The reliability of memory devices depends on a very important factor i.e. charge retention time. The retention properties estimate the length of time that the information can be stored. Fig. 4(b) shows the charge retention characteristics of the memory devices fabricated with CdTe QDs. The charge retention characteristics were measured from the time-dependent capacitance variation

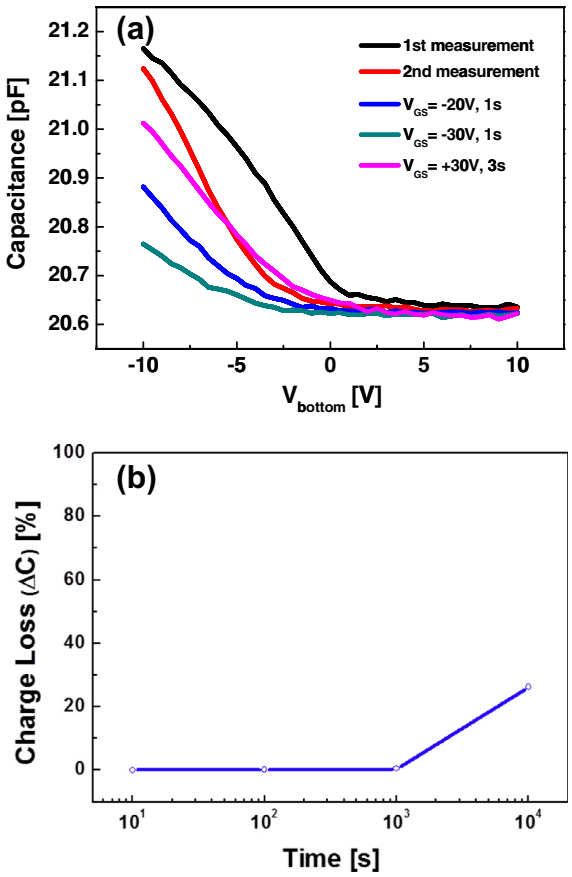

Fig. 4. (a) Capacitance change (ΔC) as a function of bottom electrode stress voltage. (b) Retention characteristics in terms of the charge loss (ΔC) after applying −30 V V_{bottom} stress voltage for 1 s.

after programming at room temperature and air environment. After programming with a V_{GS} of −30 V for 1 s, the charge loss (ΔC) was measured at V_{GS} = 0 V by sweeping the V_{GS} from +2 to −2 V in order to minimize the read commotion. The charge loss (ΔC) of the memory device slightly occurred after 10^3 s, and consequently a loss of 21.16% was observed after 10^4 s. The gradual degradation is apparently not negligible. This may be ascribed to the long-term instability of an organic semiconductor and insulator layers in the transistor memory devices; this observation demonstrates that our QD-based approach can be potentially useful for non-volatile memory applications.

4. Conclusion

The nonvolatile organic memory devices were fabricated using CdTe QDs. We studied the electrical properties of the CdTe QDs based memory device by measuring the *C–V* characteristics and retention time. Through measured *C–V* characteristic, the charging and discharging behavior of CdTe QDs as MIS structure was observed. The capacitance shift stands for hole injection in CdTe QDs as a function of increasing applied positive or negative bottom voltage stress. The memory devices using CdTe QDs exhibited a large memory window and good retention characteristics. This simple approach in processing can open up an opportunity towards the development of next-generation organic memory device.

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