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Investing the Effectiveness of Retention Performance in a Non-Volatile Floating Gate Memory Device with a Core-Shell Structure of CdSe Nanoparticles

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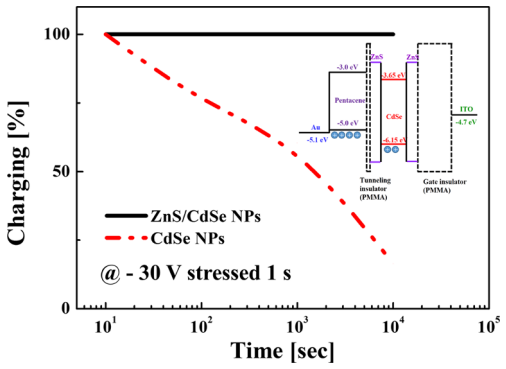
In this paper, we empirically investigate the retention performance of organic non-volatile floating gate memory devices with CdSe nanoparticles (NPs) as charge trapping elements. Core-structured CdSe NPs or core-shell-structured ZnS/CdSe NPs were mixed in PMMA and their performance in pentacene based device was compared. The NPs and self-organized thin tunneling PMMA inside the devices exhibited hysteresis by trapping hole during capacitance-voltage characterization. Despite of core-structured NPs showing a larger memory window, the retention time was too short to be adopted by an industry. By contrast core-shell structured NPs showed an improved retention time of >10000 seconds than core-structure NCs. Based on these results and the energy band structure, we propose the retention mechanism of each NPs. This investigation of retention performance provides a comparative and systematic study of the charging/discharging behaviors of NPs based memory devices.

Keywords: retention, nanoparticle, core-shell structure, organic memory, pentacene



1. INTRODUCTION

As the use of flexible electronic devices such as medical diagnostic devices, wearable devices and radio frequency identification (RFID) tags has increased explosively, extensive effort is being made for development of a non-volatile memory having high density and low cost with considerable retention time (>10 years).[1-7] Amongst the many types of non-volatile memory, flash memory, which uses a floating gate layer in a field effect transistor (FET) as a charge-trapper, is the most widely used.[8-11] Typically, the floating gate is a charge trapping site, which acts as the storage unit surrounded by SiO_2 resistive barriers. These barriers prevent carrier escape, so that the charge contained in the floating gate remains unchanged for long periods. However, despite good performance, an inorganic layer is not suitable for use in disposable and flexible electronics due to its high processing cost and brittleness. To improve device flexibility and decrease process cost, the recent trend for flash memory devices is to store information in discrete charge trapping sites using nanocrystals (NCs) with an organic insulator.[12,13]

Among various NCs, nanoparticles (NPs) are promising candidates due to easier synthesis and growth than other shapes. For this reason, many researchers have investigated various NPs, such as Cr,[14] Ag,[15] and Au,[16] in a floating-gate structure. Lee *et al.*[17] reported that the trap density of the floating gate can be controlled by accumulating Au NPs with layer-by-layer assembly. More recently, they showed that tunable memory characteristics can be obtained by using metal NPs with different electron affinities and a binary

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mixture of metal NPs. Along with these elemental metallic NPs, CdSe NPs are also promising because of their unique quantum phenomena at room temperature. While the devices based on metallic NPs have just a few fixed band-offsets, depending on the work function of the metal element, the properties of CdSe NPs are flexible. As CdSe possesses size-tunable electronic and optical properties resulting from quantum confinement, memory characteristics can be controlled based on their structure and sizes. A few studies have reported memory devices incorporating NPs to have many intriguing properties.[18,19] Unfortunately, despite the fact that organic materials have lower program/erase voltage, less damage, great endurance for write/erase cycles, and improved reliability; the retention time, an important property, was not up to the mark.[20,21] Therefore, various device structures incorporating NCs mixed with an organic material or multilayered devices have been suggested and investigated to improve retention performance.

For this reason, in this paper, we investigated the retention performance of organic non-volatile floating-gate memory devices using core-structure CdSe NPs of varying size and core-shell structure CdSe NPs. We established a retention mechanism by analyzing the energy-band structure of the device.

2. EXPERIMENTAL PROCEDURE

We fabricated the organic memory using a solution process in which CdSe NPs with different sizes and structures were employed as charge-trapping elements. The unique feature of this study is that a multilayer of self-organized CdSe NPs were formed inside the polymethylmethacrylate (PMMA) tunneling insulator, which provides a large memory window and potential multilevel charging characteristics. A distinct dependency and variation of memory characteristics on the size of CdSe NPs was observed. A wider memory window and larger charge trapping were achieved with increasing NP size.

Figure 1(a) shows a schematic illustration of the organic memory device, which comprises CdSe NPs under the pentacene layer. The metal-insulator-semiconductor (MIS) structure was fabricated on an indium-tin-oxide (ITO) coated conventional glass substrate. Firstly, a control device without CdSe NPs was fabricated by spin-coating PMMA solution on the ITO surface. The device was then baked at 160°C in a conventional oven for crystallization of PMMA insulator, which results in a 400-nm-thick PMMA insulating layer. A pentacene active layer (thickness of 70 nm) and gold top electrode was subsequently deposited on the PMMA surface using thermal evaporation. To fabricate an NP-based floating gate memory device, a mixed solution of CdSe NPs and PMMA was spin-coated on the PMMA layer. The film was baked in the oven, resulting in a NPs layer (50 nm) with

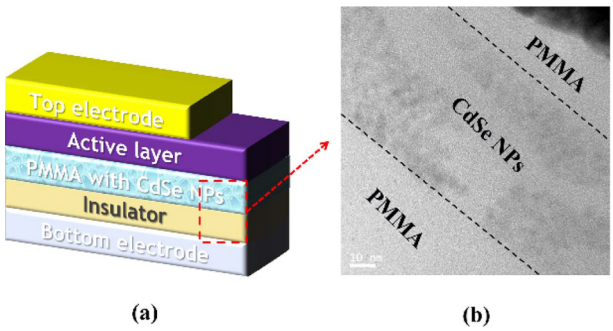

Fig. 1. (a) Schematic of the bottom-gate memory device structure using a CdSe NPs + PMMA blend as the tunneling layer for non-volatile organic memory, and (b) cross-sectional STEM image of the fabricated device featuring CdSe NPs embedded in PMMA layer.

a thin PMMA layer (25 nm), and then the semiconductor and Au electrode were serially deposited.

In this study, four types of NP differing in size distributions and structures were used: i) three core-structured CdSe NPs of 2.8, 3.3, and 4.0 nm diameter with trioctylphosphineoxide (TOPO) stabilizer were used to investigate the size effect on memory performance, and ii) a core-shell structured ZnS/CdSe NPs of ZnS capping shell was used to study the effect of structure. Figure 1(b) shows a cross-sectional scanning transmission electron microscopy (STEM) image of the fabricated device, indicating that CdSe NPs were uniformly embedded in PMMA layers without any aggregation during the blending process.

3. RESULTS AND DISCUSSION

These memory devices are based on charge-carrier transfer from the pentacene active layer to the NP layer. The transferred carriers are trapped in the NPs, resulting in individual charged islands inside the device, which consequently exhibits hysteresis behavior in capacitance-voltage (C-V). The thick PMMA layer is used to prevent the transfer of the charges between the ITO gate and the charge-trapping layer during charging/discharging operations. Therefore, the "programmed" state refers to the transfer of charge carriers (hole) from the pentacene layer to NPs upon negative bias on the gate, and the reverse operation is called the 'erased' state, in which the charge stored in the NPs is moved to the pentacene when a positive bias is applied. The programmed and erased states can be determined by the C-V characteristics upon application of bias voltage.

Figure 2(b) shows the C-V curves at 100 kHz for the device with respect to the size distribution of CdSe NPs. While the control device without CdSe NPs showed no hysteresis (Fig. 2(a)), the devices comprising CdSe NPs clearly displayed a hysteresis loop in a counter-clockwise direction upon sweeping the applied voltage at the bottom

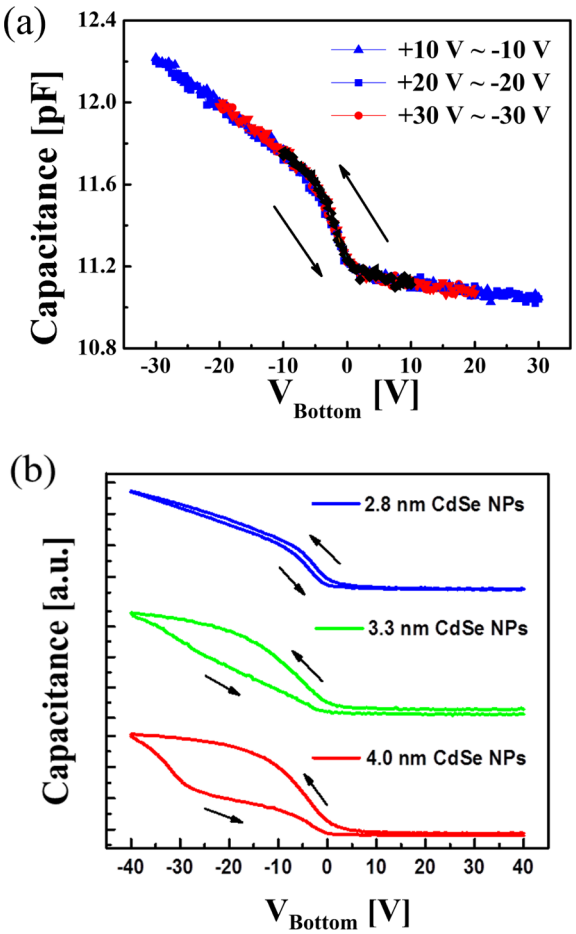

Fig. 2. The C-V characteristic of the fabricated organic memory device at different sweeping range (a) without CdSe NPs and (b) with respect to the size of CdSe NPs.

electrode between +40 and −40 V (Fig. 2(b). This indicated that a significant density of charge trapping sites exists inside the PMMA layer (and/or its interface), whereas it is negligible in the absence of NPs. The observed hysteresis during cyclic voltage sweeping was caused by the charging of CdSe NPs.

The C-V curve appeared to shift in the negative direction, indicating that the NPs layer was charged by holes due to a negative voltage. It is of importance that a greater hysteresis was clearly observed upon increasing the size of the NPs. The size-dependent capacitance of NPs can be expressed as $C_{sp}(r) = 4\pi\varepsilon_o\varepsilon_r r^2$, where ε_o is the vacuum permittivity, εr is the dielectric constant of the material surrounding the particle, and r is the radius of the NPs.[21] Therefore, the greater the size of NPs, the larger is the shift in flat band voltage, resulting in the increasing hysteresis in the C-V curve.

We analyzed the charging/discharging effects of various bias shifts in the C-V curve using CdSe NPs of different sizes as a function of amplitude of the applied positive or negative gate voltage stress. The charging/discharging effects shifted in the negative direction when a bias of −20 and −30 V was applied for 1 s. On the other hand, it shifted slightly in positive direction after erasing the memory by applying a bias of +40 V for 1 s. To evaluate size-dependent performance, memory window (ΔV), which means the difference in the critical voltage between the programmed and erased state, was measured after voltage application. Table 1 shows that the result of ΔV for the devices with 4.0, 3.3 and 2.8 nm CdSe NPs are approximately −8, −4 and 0 V at an applied voltage of −30 V, respectively. Upon applying a negative voltage, the resultant negative ΔV was attributed to the positive charge of CdSe NPs. The ΔV for the device with 4.0 nm CdSe NPs was highest due to the coulomb blockade effect. Coulomb blockade is caused by excessive charging energy (W_c), which increases as the size of nanocrystals decreases ($W_c = e^2/2C_{sp}$ and $C_{sp} = 4\pi\varepsilon_o\varepsilon_r r^2$). When $W_c >> kT$, thermal energy is no longer sufficient to overcome excessive

Table 1. Charging/discharging memory window of memory device with respect to the size of CdSe NPs.

CdSe NPs Size	2.8 nm	3.3 nm	4.0 nm
ΔV	0 V	-4 V	-8 V

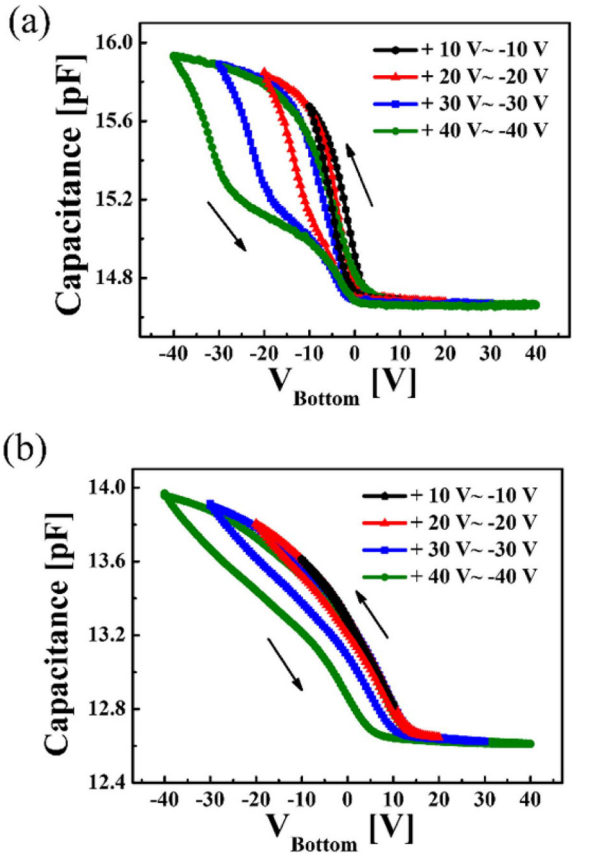

Fig. 3. The C-V characteristic of the fabricated organic memory device (a) with CdSe NPs and (b) ZnS/CdSe NPs.

charging energy. The next charge may need to occupy higher level of energy; therefore, the ΔV for the device with 4.0 nm CdSe NPs is highest among all of the devices.

The charge density Q in CdSe NPs can be estimated from $Q = C\Delta V$, where C is the capacitance between the gate and the CdSe NPs. Assuming all CdSe NPs are in the midst of PMMA layer, the charge density Q in 4.0 nm CdSe NPs can be calculated as the total charge occupied at individual CdSe NPs is 2.2×10^{11} and 4.3×10^{11} ea/cm^2 at applied voltages of −20 and −30 V, respectively.

To investigate the retention performance based on the structural effect of NPs, we additionally fabricated a memory device composed of core-shell structured ZnS/CdSe, and studied its electrical characteristics. ZnS, which covers the surround of CdSe, has a higher band gap than CdSe, resulting in the passivation of its surface. In principle, NPs passivated with inorganic shells exhibit improved tolerance to mechanical processing as well as greater optoelectronic properties. Figure 3 shows C-V curves at 100 kHz for the devices with CdSe NPs and ZnS/CdSe NPs during applied voltage sweeping. The size of the NPs used in this analysis was 4 nm. As shown in Fig. 3(a) and (b), a large hysteresis is observable in CdSe NPs with the same sweeping range, indicating that the shell of the ZnS/CdSe NPs reduces the hole-charging capability in the device. Figures 4(a) and (b) describe the energy band structure of the device with CdSe and ZnS/CdSe NPs and their accordant charging mechanism. When a sufficiently large electric field is applied (negative bias), holes can tunnel into the valence band of the CdSe NPs from the highest occupied molecular orbital (HOMO) levels of the nearby pentacene molecules. After the negative bias is removed, the tunneled holes are confined in the CdSe NPs (Fig. 4(a)). As shown in Fig. 4(b), holes are difficult to capture in the CdSe due to the energy barrier of the ZnS shell, and so the probability of the electron tunneling from the pentacene molecule to the conduction band of the CdSe NPs is decreased. The number of holes captured in the ZnS/CdSe NPs decreases due to the lower holes tunneling probability, resulting in a relatively small hysteresis in the C-V curve at the same voltage sweep.

Though the ZnS shell obstacles the hole trapping of the NPs from the pentacene layer, the large band-gap of ZnS can boost the retention of stored charge in the NPs. Charge retention characteristics of the devices with CdSe and ZnS/

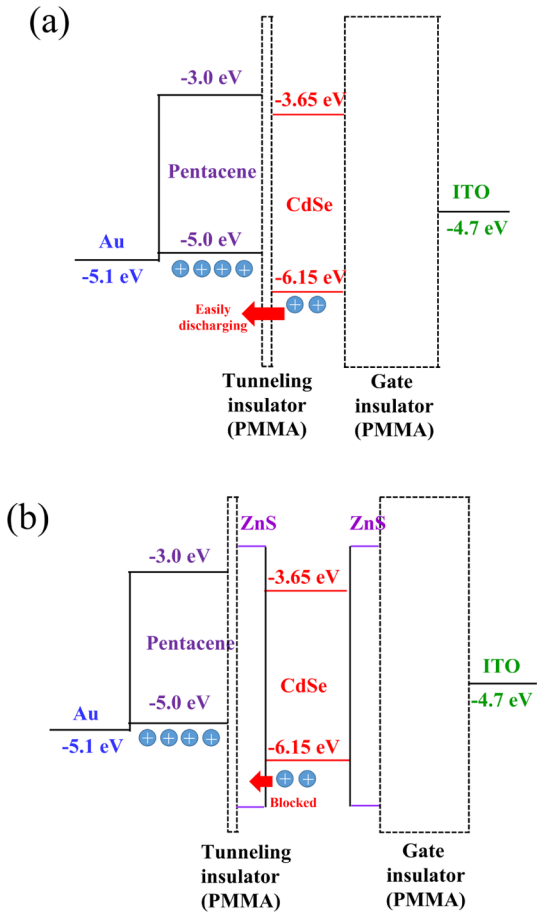

Fig. 4. The energy band schematic of memory device with (a) CdSE NPs and (b) ZnS/CdSe NPs.

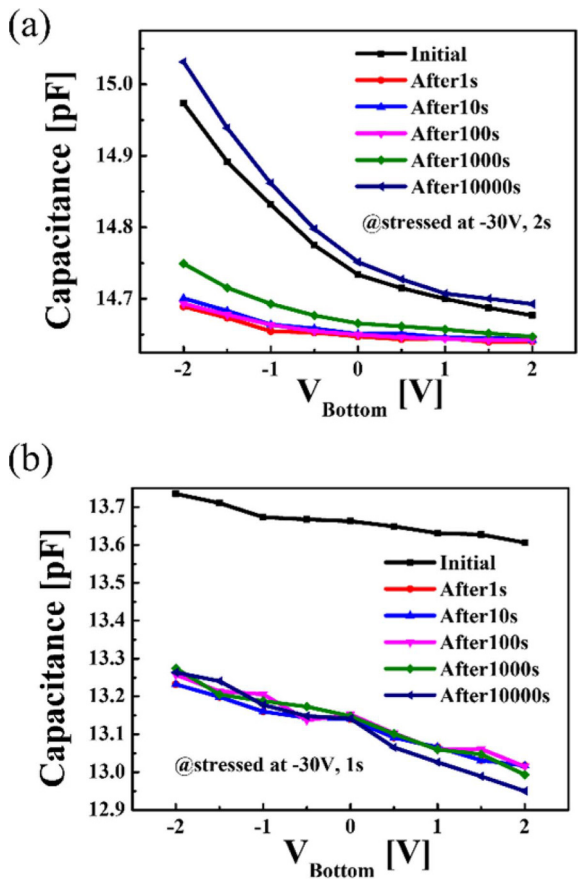

Fig. 5. Retention characteristics after applying −30 V voltage stress at the bottom electrode for 1 s: (a) CdSe NP-based device and (b) ZnS/CdSe NP-based device.

CdSe NPs were comparably measured from time-dependent capacitance change after programming at room temperature (Fig. 5(a) and (b)). After programming the device at a voltage of -30 V for 1 s, the change in the capacitance (ΔC) was measured at $V = 0$ V during sweeping V from 2 to −2 V. This measuring procedure minimizes the read disturbance. The retention performance of the device with ZnS/CdSe NPs is better than that with CdSe NPs. The capacitance of the device with CdSe NPs was 14.7 pF after programming, which changed slightly after 103 s. However, the capacitance of the device with ZnS/CdSe NPs after programming showed no significant change even after 10^4 s. The ZnS shell acted as a blocking layer for the charge dispersion.

4. CONCLUSIONS

In summary, we investigated the effects of CdSe NPs size and shell on the performance of a non-volatile organic memory device. The memory window (ΔV) widened with increasing size of the CdSe NPs. The charge retention characteristics of the device with the ZnS/CdSe NPs was clearly larger than that of the device with the CdSe NPs due to the presence of ZnS shell, and was confirmed on the basis of the C-V results and the energy-band structures. This approach provides guidelines for optimizing the size and capping shell of the NPs for different electrical applications.

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