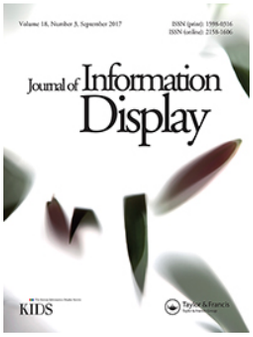

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Investigation of the drain-induced barrier lowering of low-temperature polycrystalline silicon TFTs depending on the grain configuration and channel length

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ABSTRACT

The transistor size needs to be reduced as the pixel density of the organic light-emitting diode (OLED) display increases for mobile application. Drain-induced barrier lowering (DIBL), however, hinders the further channel length reduction of low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs), which leads to severe mura of the OLED display for the low-gray level. The two-dimensional device simulation analysis showed that the potential energy barrier for the holes in the p-channel TFT decreases as the drain voltage intensifies from −1 to −10 V. The barrier lowering becomes severe as the channel length is reduced from 5 to 2 μm, but it does not have any noticeable dependency on the grain size variation from 0.3 to 0.5 μm. It was also found that the degree of DIBL varies considerably depending on the position of the grain boundary even for the same grain size, as the channel length is reduced. It was determined from the analysis that was conducted in this study that the deviation of the subthreshold current for the variation of the grain size and the grain boundary location increases 64 times as the channel length is reduced from 5 to 2 μm.

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KEYWORDS
DIBL; LTPS; TFT; grain boundary

1. Introduction

The use of organic light-emitting diode (OLED) displays for mobile phone application has been increasing of late due to their high image quality and free-form factor. For mobile OLED display application, the low-temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) is used to drive the OLED in each pixel because it has stable current–voltage characteristics and high current driving capability, which enables the integration of peripheral circuits in the narrow bezel of the display panel. As the channel area of the LTPS TFT, however, is composed of many silicon grains, the many charge traps at the grain boundaries (GB) hinder the current flow in the channel region. The electrical characteristics of the LTPS TFT are predominantly determined by the grain size and the grain boundary position in the channel [1–4]. The grain size of the polycrystalline silicon (poly-Si) film employed in OLED displays is usually between 0.3 and 0.5 μm when it is produced through excimer laser annealing (ELA). As the grain size is comparable to the channel dimension (several microns), the variation of the grain boundary position, which is randomly determined during the laser annealing process, results in the poor uniformity of the electrical characteristics of the LTPS TFT especially between the neighboring pixels [5–6]. To overcome the non-uniform characteristics of the LTPS TFT and to realize uniform brightness, a compensation circuit is used in each pixel of the commercial OLED display. The compensation circuit adjusts the gate-to-source bias (V_{GS}) of the OLED-driving TFT according to its threshold voltage value.

As the pixel density gets higher for mobile applications, the TFT size should also be reduced. The drain current is seriously increased by the strong drain bias (V_{DS}) in the subthreshold region with decreasing channel length due to drain-induced barrier lowering (DIBL), as shown in Figure 1. The degree of DIBL also differs between the neighboring TFTs, but it is impossible to compensate for the current deviation due to DIBL, even through the compensation circuit, because the compensation process proceeds from on-state to the threshold condition. As the current level where the compensation process stops is above 1 nA, the current deviation in the sub-nA range due to DIBL cannot be corrected.

The DIBL of the p-channel LTPS may be explained by the schematic diagram shown in Figure 2. In small and

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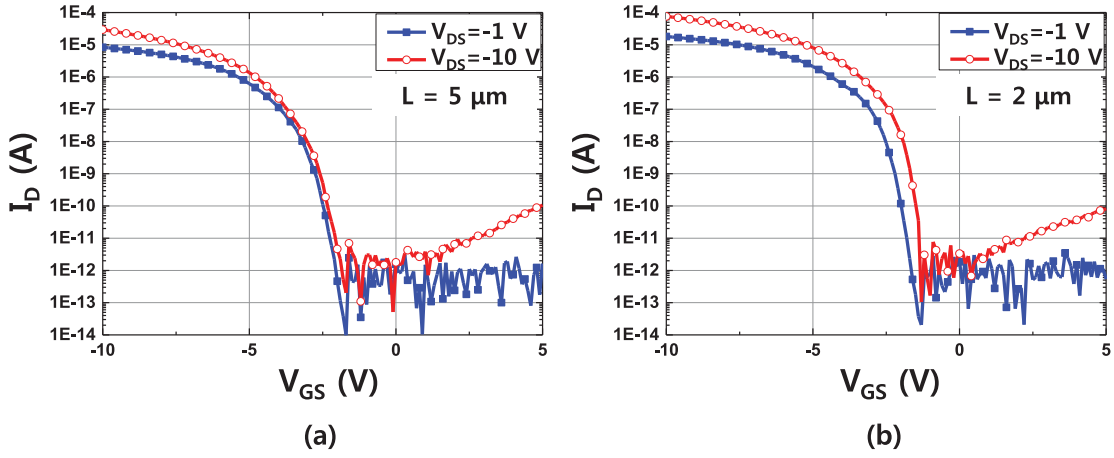

Figure 1. Transfer characteristics of the long- and short-channel LTPS TFTs: (a) $L = 5$ μm; and (b) $L = 2$ μm.

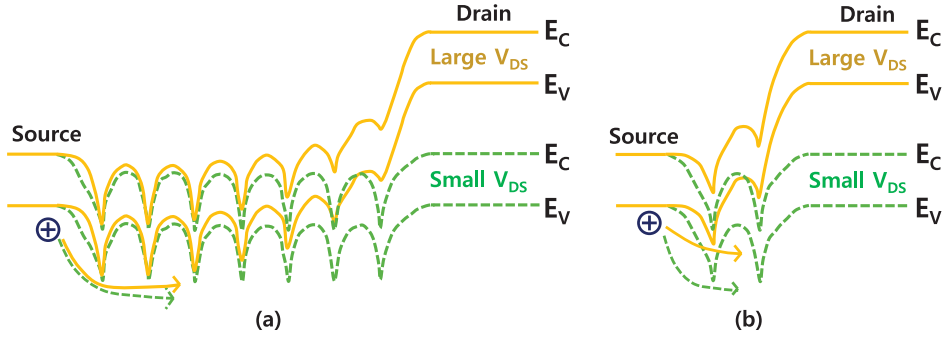

Figure 2. Energy band diagrams of the LTPS TFTs: (a) long channel; and (b) short channel.

large V_{DS} cases for long-channel TFTs, the GB energy barrier height near the source is not significantly different, but it is considerably reduced for short-channel TFTs as the V_{DS} increases [4]. As a result, the subthreshold current may seriously increase for a large V_{DS}. In this article, how the subthreshold current of the p-channel LTPS TFT varies when the grain size and the position of the GB change is reported with the aid of the two-dimensional (2D) 'ATLAS' technology computer-aided design (TCAD) software from SILVACO.

2. TCAD modeling of LTPS TFT

Figure 3 shows an example of the cross-sectional structure of the LTPS TFTs used in the simulation analysis in this study. As the channel length is 3 μm and the grain size is 0.5 μm, there are seven GB in the channel region between the source and the drain. The poly-Si film is subdivided into three regions: the poly-Si grain, the grain boundary, and the Si–SiO_2 interface. Each region has a different trap state density. The width of the grain boundary is assumed to be 4 nm. The mesh size of the grain boundary in the simulation is 1 nm in the horizontal direction. The device parameters that were used in the

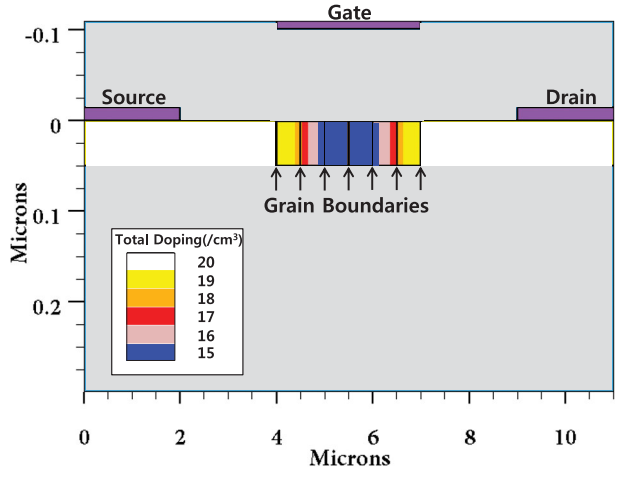

Figure 3. Structure of the LTPS TFT for the TCAD simulation when the channel length was 3 μm and the grain size was 0.5 μm.

TCAD simulations are listed in Table 1. In the 2D simulation, the channel width of the device was fixed at 1 μm, but the channel lengths were varied from 2 to 5 μm. The thicknesses of the gate oxide and poly-Si film were 100 and 50 nm, respectively, which are the typical values for the LTPS TFT in OLED displays. The doping concentration in the source and drain region was $1 \times 10^{20}/cm^3$,

Table 1. Device parameters used in the TCAD simulation.

Device parameters	Symbol (units)	Value
Channel length	L (μm)	2, 3, 4, 5
Channel width	W (μm)	1
Gate oxide thickness	t_{ox} (nm)	100
Polysilicon thickness	t_{si} (nm)	50
Si–SiO_2 interface thickness	t_{int} (nm)	1
Source and drain dopant density	N_A (cm^{-3})	1×10^{20}
Characteristic length of the lateral dopant diffusion	char (μm)	0.217
Fixed oxide charge density at the Si–SiO_2 interface	qf (cm^{-2})	1.5×10^{11}

and the channel region was also doped as p-type with a $1 \times 10^{15}/cm^3$ dopant concentration.

For the modeling of the measured characteristics of the p-channel LTPS TFT using the device structure in Figure 3, the trap state parameters of the three regions of the poly-Si listed in Table 2 were optimized. The density of the fixed oxide charge at the Si–SiO_2 interface and the characteristic length of the lateral dopant diffusion at the source/drain junctions were chosen to be $+1.5 \times 10^{11}/cm^2$ and 0.217 μm, respectively, to fit the measured characteristics.

The trap state density of the poly-Si is given by

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E),$$

where $g_{TA}(E)$ is the density of the acceptor-like tail states in the upper half of the bandgap, $g_{TD}(E)$ is the density of the donor-like tail states in the lower half of the bandgap, and $g_{GA}(E)$ and $g_{GD}(E)$ are the densities of the acceptor- and donor-like deep states, respectively. The detailed equations for the trap state density are shown in [6]. The values of the trap state parameters for the three regions of poly-Si were determined to fit the measured characteristics regardless of the channel length variation from 2 to 5 μm, and also for the different grain sizes (0.3 and 0.5 μm). The Shockley–Read–Hall recombination and the Lombardi mobility model were used in the simulation. The impact ionization was also taken into consideration [7].

Figures 4 and 5 show the results of the TCAD modeling with the parameters listed in Tables 1 and 2 in comparison with the measured TFT characteristics for the 2 and 5 μm channel lengths. The solid lines are the characteristics of the TCAD model, and the dashed lines are those of the measured TFT. For the TCAD model, two grain sizes, 0.3 and 0.5 μm, are assumed because the typical grain size of ELA poly-Si is between 0.3 and 0.5 μm. The transfer characteristics of the model TFTs are in good accordance with the measured characteristics regardless of the channel length. The small difference between them

Table 2. Poly-Si trap state parameters used in the TCAD simulation.

Poly-Si trap state parameters	Symbol (units)	In-grain	Grain boundary	Si–SiO_2 interface
Density of the acceptor-like tail states	N_{TA} (cm^{-3}•eV^{-1})	4×10^{21}	7×10^{21}	6×10^{21}
Density of the donor-like tail states	N_{TD} (cm^{-3}•eV^{-1})	2×10^{20}	2×10^{21}	3×10^{20}
Characteristic decay energy of the acceptor-like tail states	W_{TA} (eV)	0.01	0.03	0.01
Characteristic decay energy of the donor-like tail states	W_{TD} (eV)	0.05	0.06	0.05
Density of the acceptor-like Gaussian states	N_{GA} (cm^{-3}•eV^{-1})	1×10^{16}	$1\ 10^{18}$	$1\ 10^{18}$
Density of the donor-like Gaussian states	N_{GD} (cm^{-3}•eV^{-1})	$3\ 10^{16}$	1×10^{18}	$2\ 10^{17}$
Peak energy of the Gaussian distribution of the acceptor-like deep states	E_{GA} (eV)	0.4	0.4	0.4
Peak energy of the Gaussian distribution of the donor-like deep states	E_{GD} (eV)	0.4	0.4	0.4
Characteristic decay energy of the acceptor-like Gaussian states	W_{GA} (eV)	0.35	0.35	0.35
Characteristic decay energy of the donor-like Gaussian states	W_{GD} (eV)	0.2	0.3	0.29

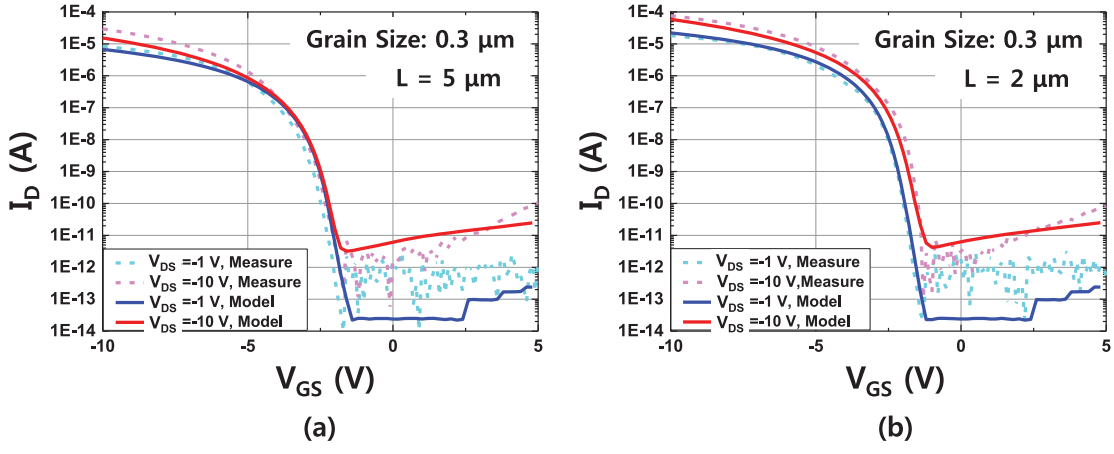

Figure 4. Comparison of the measurement results and the TCAD model with a 0.3 μm grain size: (a) $L = 5$ μm; and (b) $L = 2$ μm.

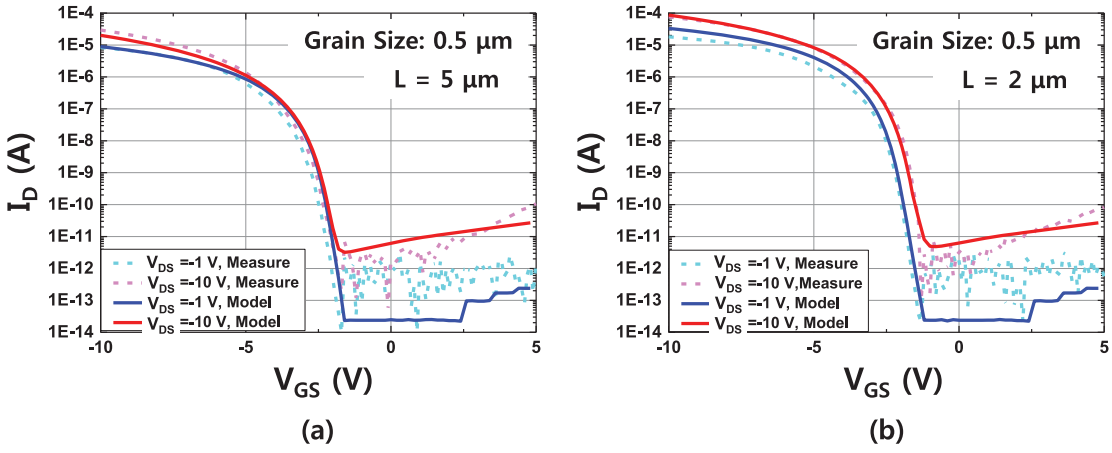

Figure 5. Comparison of the measurement results and the TCAD model with a 0.5 μm grain size: (a) $L = 5$ μm; and (b) $L = 2$ μm.

may be attributed to the non-uniform grain size in the real TFT.

3. Results

Figure 6 shows the valence band edge (E_V) of the LTPS TFT channel region when the grain size is 0.5 μm and the channel lengths are 5 (a) and 2 μm (b). The energy band diagram is drawn along the horizontal line 1 nm below the Si–SiO_2 interface. The source-side edge of the gate electrode is located at the 4 μm position for both devices. The blue line represents the E_V for $V_{DS} = -1$ V, and the red line represents the E_V for $V_{DS} = -10$ V. The gate-to-source biases (V_{GS}) of −2.0 V for the 2-μm-channel-length device and of −2.4 V for the 5-μm-channel-length device were chosen to put the devices in the deep subthreshold region. The criterion that was used for determining the V_{GS} for the deep subthreshold condition was to find the V_{GS} value for which the drain current was 200 pA at $V_{DS} = -1$ V. The barrier height for the hole carriers was defined as the lowest value of E_V, as shown in Figure 6. The barrier height tends to appear at the grain boundary for long-channel devices whereas it may not appear at the grain boundary for short-channel devices because the distance between the GB is almost comparable to the channel length. For the 5-μm channel length, the barrier height difference between $V_{DS} = -1$ V and $V_{DS} = -10$ V is negligible, as shown in Figure 6(a), but it is remarkably reduced for the 2-μm channel length as V_{DS} intensifies from −1 to −10 V, as shown in Figure 6(b). As a result, a considerable increase in hole injection over the reduced barrier height is expected.

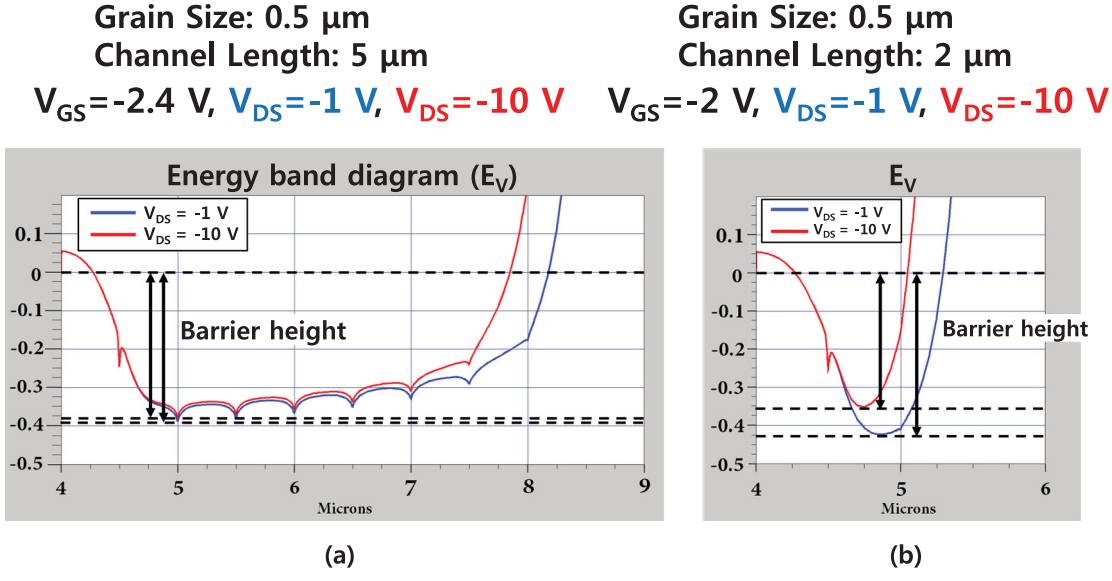

Figure 6. Energy band diagram (E_V) of the TFT channel region with a 0.5 μm grain size for $V_{DS} = -1$ V and $V_{DS} = -10$ V: (a) $L = 5$ μm; and (b) $L = 2$ μm.

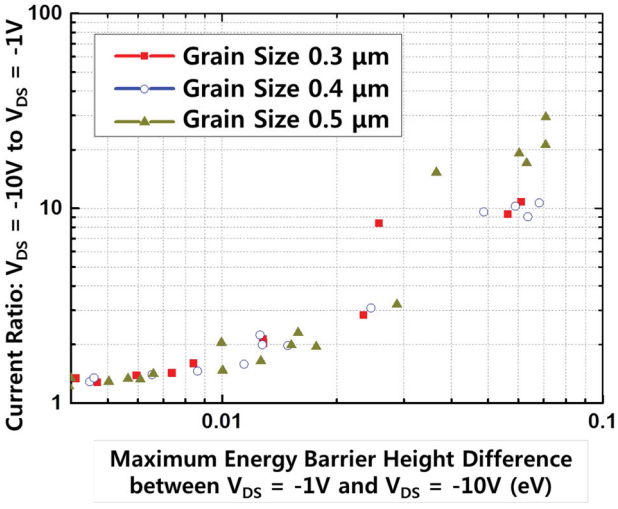

Figure 7. Current ratio between $V_{DS} = -1$ V and $V_{DS} = -10$ V vs. maximum energy barrier height difference depending on the grain size. The data for the different grain boundary locations with ±0.1 and ±0.2 μm shifts are included.

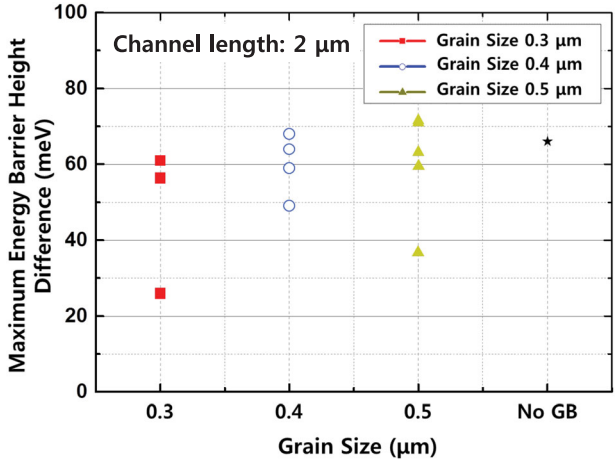

Figure 8. Maximum energy barrier height difference depending on grain size when channel length is 2 μm. Data for different grain boundary location with ±0.1 μm and ±0.2 μm shift are included.

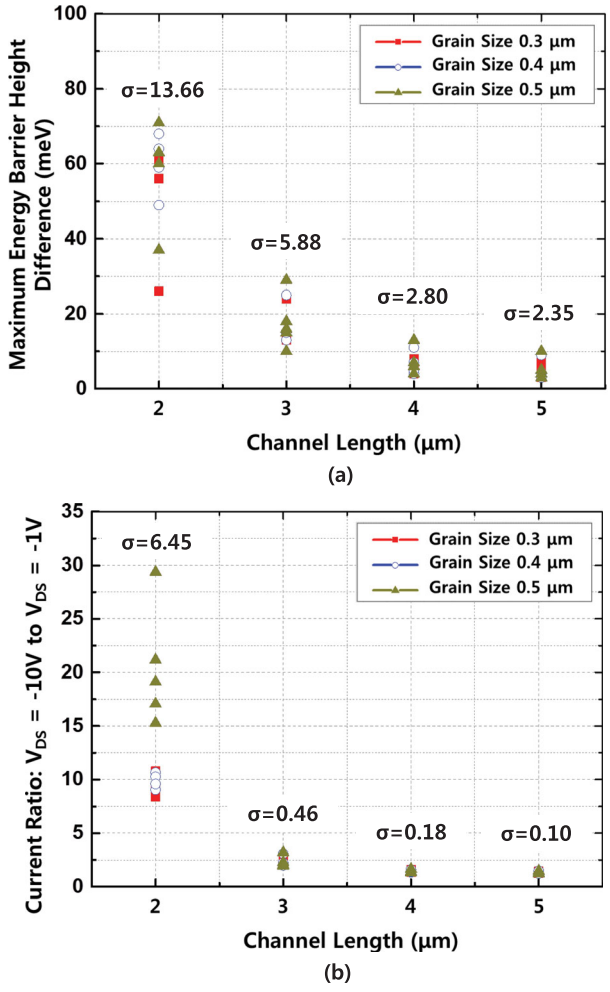

Figure 9. (a).The deviation of maximum energy barrier height difference depending on channel length. Data for different grain boundary location with ±0.1 μm and ±0.2 μm shift are included. (b). The deviation of current ratio for $V_{DS} = -10$ V to $V_{DS} = -1$ V depending on channel length.

The location of the GB is randomly determined during the ELA process. As such, the position of the grain boundary in the channel region was varied by 0.1 μm steps in the TCAD simulation. For example, the position of all the GB was shifted by 0.1 μm toward the drain (+0.1 μm) and also by 0.1 μm toward the source (−0.1 μm) for the 0.3-μm grain size. The simulation results of all these conditions are shown in Figures 7–9.

Figure 7 shows the relations between the barrier lowering and the current increase as V_{DS} intensifies from −1 to −10 V. All the simulation results for the channel length variation from 2 to 5 μm, for the grain size variation from 0.3 to 0.5 μm, and for the grain boundary position variation are included. It is shown that the current increase is solely attributed to the barrier height reduction. The grain size variation does not seem to make any noticeable difference because the data for the different grain sizes overlap on the graph. Figure 8 also shows that the degree of DIBL has no noticeable dependence on the grain size for the 2-μm-channel-length devices. It should be noted, however, that the effect of the different grain boundary position is very large. The barrier height decrease for the no-grain-boundary case is not very different from those in the other cases with several GB. To find the effect of the channel length, the average values of the barrier height decrease in Figure 7 for each channel length were calculated, and the results are listed in Table 3. It is shown that the degree of DIBL certainly increases as the channel length decreases,

Table 3. Average DIBL for $V_{DS} = -10$ V depending on the grain size and channel length.

$V_{GS}@I_D = 200$ pA, $V_{DS} = -1$ V		Channel length 2 μm	3 μm	4 μm	5 μm
Grain size	0.3 μm	48 meV	16 meV	6 meV	5 meV
	0.4 μm	60 meV	16 meV	7 meV	5 meV
	0.5 μm	60 meV	17 meV	7 meV	5 meV
	No grain boundary	66 meV	14 meV	5 meV	4 meV

but the effect of the grain size variation is not clearly observed.

The grain size of the ELA poly-Si TFT may vary even in a single device. Moreover, the position of the grain boundary can be different from one device to another, even for the neighboring pixels. Figure 9 shows how the subthreshold current varies due to the random distribution of the poly-Si grains as the channel length decreases. The standard deviation of the subthreshold current increase ratio for the above-mentioned bias conditions increases anomalously from 0.10 to 6.45 as the channel length decreases from 5 to 2 μm. This large current deviation leads to severe mura in the OLED display because the compensation circuit cannot correct the deviation of the subthreshold characteristics.

4. Conclusion

The 2D TCAD simulation of the p-channel LTPS TFTs showed that the subthreshold current seriously increases due to DIBL as the channel length decreases from 5 to 2 μm. The maximum potential barrier may appear inside the grain as well as the grain boundary as the channel length decreases. The degree of DIBL does not have any noticeable dependency on the grain size variation from 0.3 to 0.5 μm. On the contrary, it varies remarkably depending on the position of the grain boundary. The standard deviation of the barrier lowering for various grain sizes and grain boundary locations increases from 2.35 to 13.66 meV, and that of the subthreshold current ratio between $V_{DS} = -1$ V and $V_{DS} = -10$ V increases 64 times as the channel length is reduced from 5 to 2 μm. The non-uniform DIBL characteristics of the short-channel LTPS TFT are attributed to the random distribution of the GB in the channel region rather than to the grain size variation. The channel of the LTPS TFT should be long enough to suppress the harmful effect of the non-uniform DIBL characteristics on the display quality of the OLED panel.

Disclosure statement

No potential conflict of interest was reported by the authors.

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