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IGZO TFT gate driver circuit with large threshold voltage margin☆

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ABSTRACT

This paper proposes a new gate driver circuit using depletion mode a-IGZO TFTs. The proposed gate driver circuit can prevent Q node, the gate node of pull-up TFT, from discharging during the output pulse duration. For that purpose, our circuit applies sufficient negative gate-to-source bias (V_{gs}) to the switch TFTs connected to the Q node during that time. Consequently, the leakage current through them is suppressed even though they have a negative threshold voltage (V_{th}). The proposed circuit has eleven transistors and two capacitors and it requires only two clock signals, which enables us to adopt the circuit at minimum extra cost. It works properly even when V_{th} is as low as −7.1 V. The normalized power consumption of the proposed circuit is also lowered compared with the previously reported circuits when the transistor has negative V_{th}. The power consumption of the proposed circuit for V_{th} of −5 V increases only nine times that for V_{th} of 3 V.

1. Introduction

Amorphous indium gallium zinc oxide thin film transistors (a-IGZO TFTs) have become a suitable candidate for various flat-panel displays due to high mobility and uniform electrical properties as compared to amorphous Si:H [1–3]. Due to the high mobility of a-IGZO TFTs, the active matrix liquid crystal displays (AMLCDs) using a-IGZO TFTs are able to provide high frame frequency and high resolution. The a-IGZO TFTs are also used for the backplane of active matrix organic light emitting diode (AMOLED) displays. However, the a-IGZO TFTs have a problem of negative threshold voltage [4–10]. The leakage current through these TFTs in a conventional gate driver circuit induces anomalously large power consumption [11–13]. Therefore, studies for the gate driver circuit that can be operated in the depletion mode would be useful for a-IGZO TFT display [14]. In this paper, we present a new gate driver using depletion mode a-IGZO TFTs. The proposed gate driver circuit can prevent the discharging of Q node, the gate node of pull-up TFT, for the output pulse duration. Negative V_{gs} is applied to the switch TFTs connected to the Q node during that time so as to prevent the leakage current through them even though they have a negative V_{th}. The proposed circuit has a very simple structure compared to those in previously reported papers. The proposed circuit has large V_{th} margin for circuit operation. The normalized power consumption of the proposed circuit decreases as the V_{th} increases in the negative direction, when compared with gate driver circuits in previously reported papers.

2. Proposed gate driver circuit and operation

2.1. Problems of conventional gate driver circuit

The conventional gate driver circuit using depletion mode a-IGZO TFT has two problems. The first problem is the voltage drop of Q node during the output pulse duration. Whenever this phenomenon gets severe, the gate driver circuit does not work. To be more specific, during the pre-charging and the output pulse durations in a conventional circuit (Fig. 1), the QB node has very low voltage level (VSS) and the value of V_{gs} of T3 transistor is close to zero. If the conventional circuit has depletion mode TFTs, T3 transistor is not completely turned off. As a result, a considerable amount of leakage current flows through. The second problem is high power consumption due to the leakage current of the inverter circuit composed of T4 and T5 transistors that control the QB node. In the holding duration, the root mean square (RMS) value of the low Q node voltage is about −4.95 V. Thus, the V_{gs} of T5 transistor is set to about 0.05 V based on RMS voltage of Q node. The charge in the QB node is discharged to the VSS node by the T5 transistor in an unusually turned on state. The QB node is then charged from the VDD node by T4 transistor. Thus, the power consumption of the conventional gate driver circuit sharply increases as negative V_{th} increases due to the leakage current of the inverter circuit. This phenomenon also occurs in the circuits in previously published papers [3,12].

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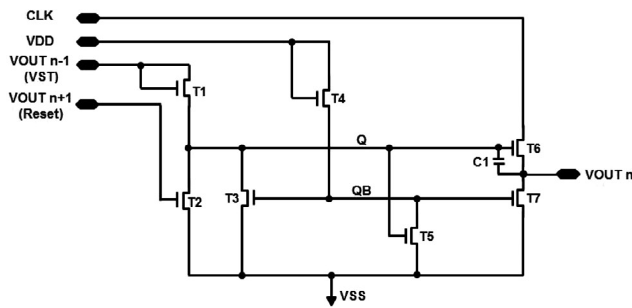

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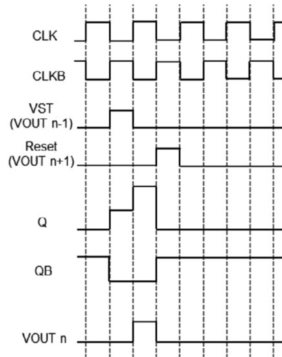

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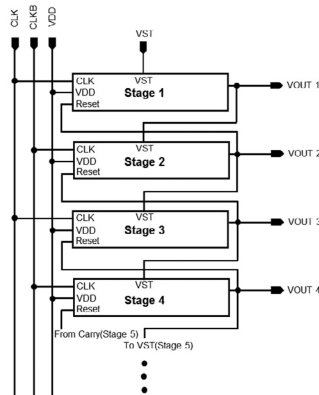

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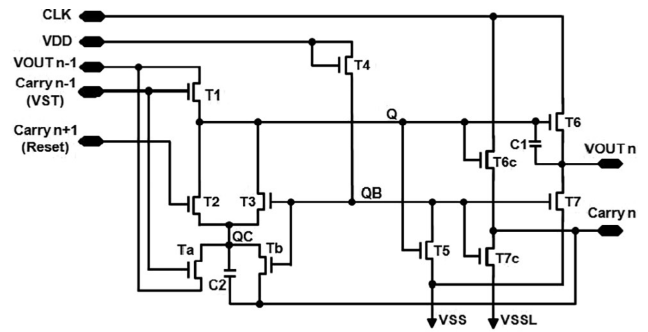
Fig. 1. The conventional gate driver circuit: (a) 1 stage circuit unit, (b) timing diagram, and (c) block diagram.

2.2. Proposed gate driver circuit

Fig. 2 shows the proposed depletion mode a-IGZO TFT gate driver circuit, timing diagram, and block diagram. The 1 stage unit of the proposed circuit is composed of eleven transistors and two capacitors as shown in Fig. 2(a). The circuit has two clock signals, namely CLK and CLKB. Three sources of DC voltages are applied to this circuit: VSS of −5 V, VSSL of −13 V, and VDD of 28 V. It has three operation durations: pre-charging duration, output pulse duration, and holding duration. We have proposed two new concepts in this circuit. According to the first concept, the circuit introduces a new node called QC, as shown in Fig. 2(a) and (b). In the circuit, the discharging of the Q node caused by the leakage current of T2 and T3 transistors during the output pulse duration can be prevented due to the addition of QC node. In [12], it is reported that a similar QC node can be charged to the VDD node and discharged to the VSSL node using transistor switching. This circuit path is a leakage current path, accompanied by a consequent power consumption increase. However, the QC node of our proposed circuit is charged by Ta transistor, boosted by the C2 capacitor, and discharged by Tb transistor. Thus, our circuit has no leakage current path. In the



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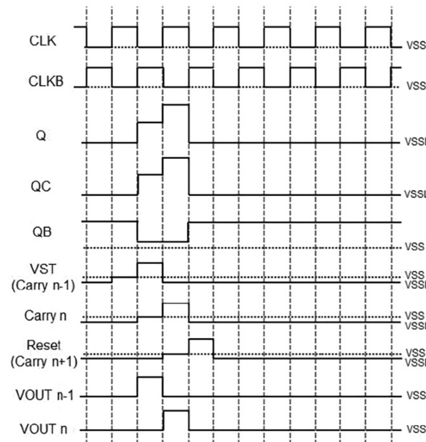

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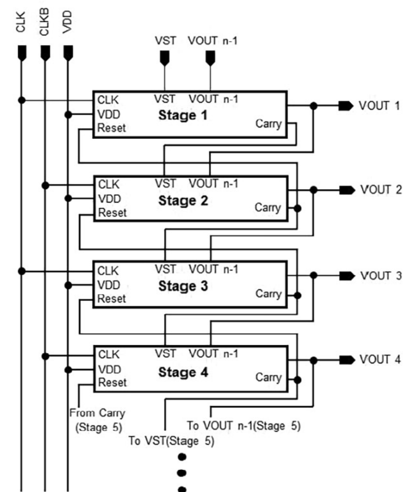

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Fig. 2. The proposed gate driver circuit: (a) 1 stage circuit unit, (b) timing diagram, and (c) block diagram.

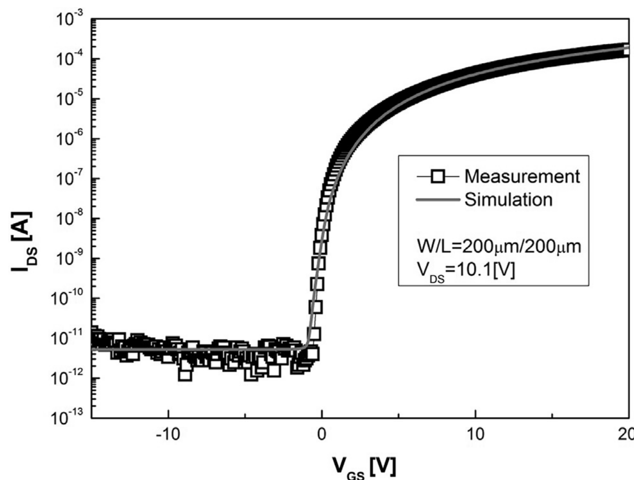


Fig. 3. The measured and simulated transfer characteristics of depletion mode a-IGZO TFT.

pre-charging duration, T1 transistor and Ta transistor are turned on by the VST signal to charge the Q and QC nodes. In the output pulse duration, the Q node is boosted by C_{gd} of T6 transistor. At the same time, the QC node is boosted by C2. Because the QC node is driven in a fashion similar to the Q node in the output pulse duration, V_{gs} of T2, T3, Ta, and Tb transistors connected with the QC node have a negative voltage. As a result, these transistors are completely turned off. Therefore, the proposed gate driver circuit can prevent the discharging of the Q node caused by the leakage current during the output pulse duration. The gates of T1 and Ta transistors are connected to Carry n-1 node, and the drain of T1 and the source of Ta are then connected to VOUT n-1 node so that $V_{gs} < 0$ V can be applied to them. The source of Tb transistor is connected to Carry n node for the same reason. In the conventional circuit, the Q node voltage drop decreases as the C1 capacitance increases. The leakage current from the Q node to the VSS node is considerably higher in the conventional circuit than that of the proposed circuit, therefore a large C1 value is needed in the conventional circuit. It is not possible for C1 to have a very large value due to

Table 1
Design parameters of the conventional and proposed gate driver circuit.

Conventional Circuit		Proposed Circuit	
T1,T6 L	5 μm	T1, T6, T6c L	5 μm
T2, T3, T4, T5, T7 L	20 μm	T2, T3, T4, T5, T7, T7c, Ta, Tb L	20 μm
T1W	15 μm	T1 W	15 μm
T2, T3, T4W	5 μm	T2, T3, Tb W	30 μm
T5 W	50 μm	T4, T6c, Ta W	5 μm
T6 W	75 μm	T5 W	50 μm
T7 W	100 μm	T6 W	70 μm
C1 Capacitance	50 pF	T7 W	90 μm
CLK, CLKB Voltage	−5 to 28 V	T7c W	10 μm
CLK Duty Ratio	50 %	C1 Capacitance	2 pF
VSS	−5 V	C2 Capacitance	1 pF
CLK Frequency	25 kHz	CLK, CLKB voltage	−5 to 28 V
		CLK Duty Ratio	50 %
		VDD	28 V
		VSS	−5 V
		VSSL	−13 V
		CLK Frequency	25 kHz

L = TFT Length, W = TFT Width.
CLK Frequency 25 kHz = Line Time 20 μs (HD Resolution, Frame Frequency 60 Hz).

large circuit area requirement. In the second concept, the V_{gs} of the driving T5 transistor of the inverter is less than zero using two low-voltage supplies (VSS and VSSL), as shown in Fig. 2(a). In the holding duration, T3 and Tb transistors are turned on by the QB node voltage to discharge the Q node. Then, T5 transistor is turned off by the Q node voltage to charge the QB node. In this paper, the V_{gs} of the driving T5 transistor of the inverter circuit for the QB node operation is less than zero using the two low-voltage supplies. The gate and source voltages at the moment of turning off of T5 are equal to the Q node RMS voltage of −12.6 V and the VSS of −5 V, respectively. The V_{gs} of T5 transistor has the value of −7.6 V. It is possible to decrease the leakage current from the QB node to the VSS node if the T5 transistor is completely turn off. The measured and simulated transfer characteristic of the depletion a-IGZO TFT are shown in Fig. 3. The transfer characteristics show a threshold voltage of −0.35 V and a field-effect mobility of 31 cm^2/(V s). Assuming a video graphics HD (1366 × 768) display panel, we attached a 4 kΩ resistor and a 100 pF capacitor to each output node to emulate the gate line load for the purpose of simulation. Table 1 shows the design parameters of the conventional and the proposed gate driver circuit. In order to simulate the driving characteristics and negative V_{th} limit for circuit operation, we simulated the last 10 stages in a 768 stage gate driver. It should be noted that the preceding 758 stages were emulated using an equivalent circuit of a resistor and a capacitor and the power consumption simulation was simulated based on 768 stages.

3. Results and discussions

The proposed circuit has a very simple structure compared to those in previously reported papers. The gate driver circuit reported in [12] has seventeen transistors and two low-voltage supplies per stage. And, the circuit reported in [14] has fifteen transistors, seven capacitors, and three low-voltage supplies per stage. In comparison, the proposed circuit has eleven transistors and two capacitors and it requires only two clock signals, which enables us to adopt the circuit at minimum extra cost. We used SmartSpice to simulate the operation of both the conventional and the proposed gate driver circuits. The negative V_{th} limit for circuit operation is simulated by a variable C1 value (3–50 pF) for the conventional circuit and fixed C1 and C2 values (C1 = 2 pF, C2 = 1 pF) for the proposed circuit. The negative V_{th} limit for circuit operation is also analyzed by a variable CLK frequency. We analyzed the difference in the power consumption between the circuits in previously published paper [11] and the proposed circuit. Fig. 4 shows the simulated voltage waveforms of the conventional and proposed gate driver circuits with a transistor V_{th} of 0.5 V and non-depletion mode of transistor operation. In this case, the waveform results show conventional operation without any problems during all three operation durations. Fig. 5 shows the simulated voltage waveforms of the conventional and proposed gate driver circuits with a transistor V_{th} of −2.9 V and depletion mode of transistor operation. In the Q node bootstrapping step, the conventional gate driver Q node gets discharged due to the current leaking from the Q node to VSS, as shown in Fig. 5(a). On the other hand, there is not discharging of Q node in the proposed circuit, as shown in Fig. 5(c). Fig. 5(b) shows the distortion of the VOUT waveform of the conventional circuit, whereas Fig. 5(d) shows a very good VOUT waveform of the proposed circuit. The QC node voltage is 8.6 V in the pre-charging step and 26.5 V in the bootstrapping step, as shown in Fig. 5(c). Thus, T2, T3, Ta, and Tb transistors which are connected to the QC node are completely turned off. Hence, the leakage current from the Q node to VSSL is prevented. In the conventional circuit, the Q node is charged to 20.3 V in the pre-charging step and is discharged from 44.5 V to 22.2 V in the bootstrapping step, as shown in Fig. 5(a). This is because V_{gs} of T3 transistor is about 2.5 V and T3 transistor with V_{th} of −2.9 V is not completely turned off. The Q node voltage drop decreases as the C1 value of the conventional

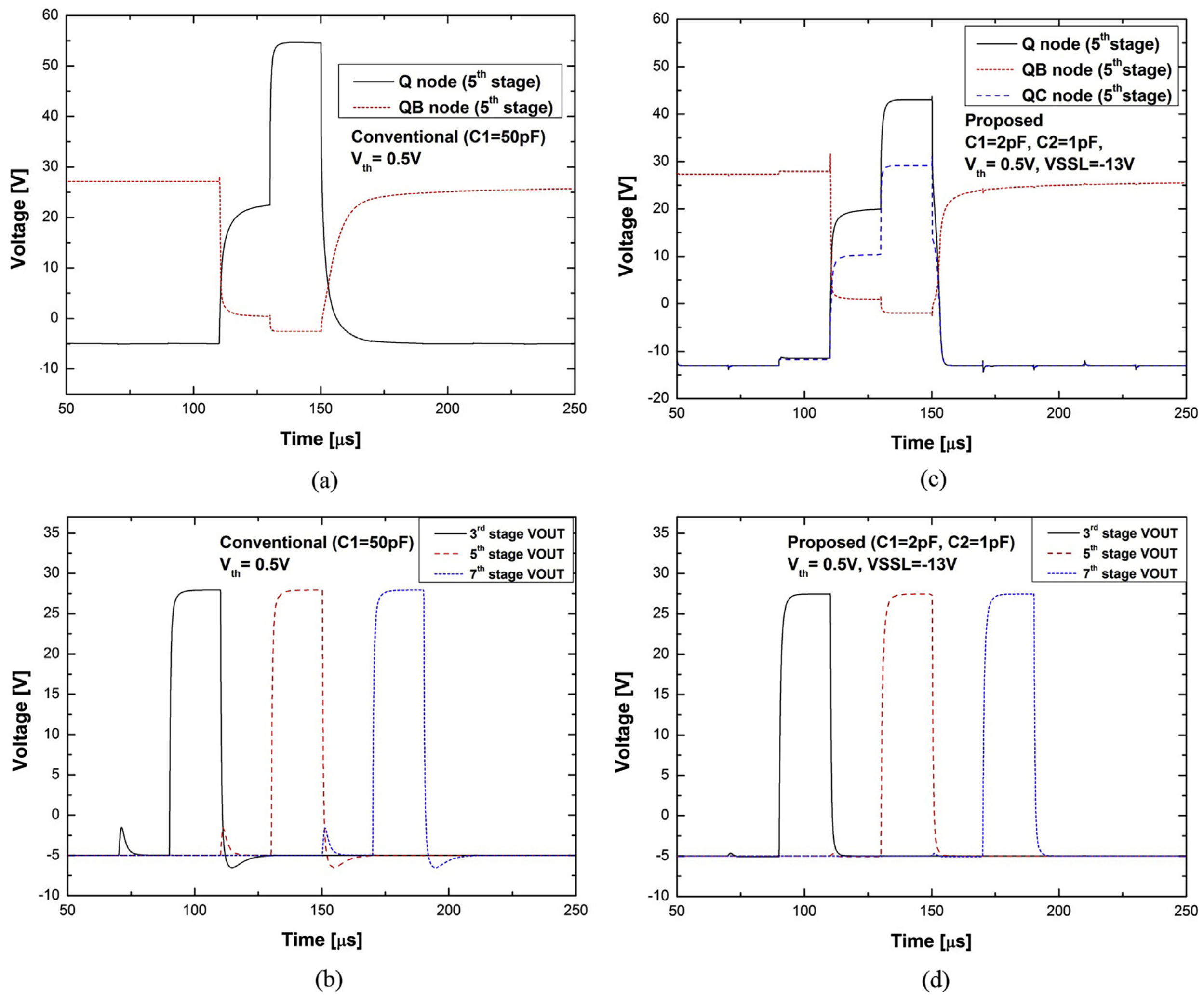


Fig. 4. The simulated voltage waveforms (V_{th} = 0.5 V): (a) conventional circuit Q and QB for 5th stage, (b) conventional circuit 3rd, 5th, and 7th stage VOUT, (c) proposed circuit Q, QB, and QC for 5th stage, and (d) proposed circuit 3rd, 5th, and 7th stage VOUT.

increases, as shown in Fig. 6 (a), because the total capacitance of the Q node increases. When the C1 value of the conventional circuit is 50 pF, the result values of negative V_{th} limit for circuit operation is −2.9 V, as shown in Fig. 6(a). However, the negative V_{th} limit of the proposed circuit with C1 = 2 pF and C2 = 1 pF has a very large value of −7.1 V at VSSL = 13 V and VSS = −5 V. Our proposed circuit has a very small capacitor and thus, has a significantly improved negative V_{th} limit for circuit operation when compared with conventional circuit. The parameter VSSL is applied only in the proposed circuit. Fig. 6(b) shows the relationship between negative V_{th} limit for circuit operation and VSSL. When the VSSL voltage is applied in the range of -15 V to −10 V, the resulting values range of negative V_{th} limit is −8.0 V to −5.4 V, as shown in Fig. 6(b). T1 transistor of the proposed circuit is connected with VOUT n-1 and Carry n-1. The low voltage values of VOUT n-1 and Carry n-1 are VSS and VSSL, respectively. Thus, V_{gs} of T1 transistor is the voltage difference between VSS and VSSL. V_{gs} of T1 increases in a negative direction as VSSL increases in a negative direction at VSS of −5 V. Thus, the Q node voltage drop decreases as the voltage difference between VSS and VSSL increases. Fig. 6(c) shows the relationship between CLK frequency and the negative V_{th} limit for circuit operation. The negative V_{th} limit of both the conventional circuit and the proposed circuit decrease as the CLK frequency decreases. When the CLK frequency is applied at 50 and 1.4285 kHz, the negative V_{th} limit of the conventional circuit with C1 of 50 pF are −3.7 V and −2.25 V respectively, and the negative V_{th} limit of the proposed circuit with C1 of 2 pF and C2 of 1 pF are −7.35 V and −6.95 V, respectively. The discharging time of the Q node voltage decreases as the CLK frequency increases. Thus, negative V_{th} limit for circuit operation is improved correspondingly. In the holding duration, the QB node voltage severely drops to the RMS value of 19.9 V, as shown in Fig. 5(a). For the QB node control in the conventional circuit, the V_{gs} of T5 transistor which drives the inverter, is 0.05 V based on the RMS voltage of the Q node. Because V_{th} is −2.9 V, the T5 transistor is not completely turned off. The severe voltage drop at the QB node of the conventional circuit is caused by the leakage current of the T5 transistor. In contrast, for the QB node control in the conventional circuit, the V_{gs} of T5 transistor which drives the inverter, is −7.6 V based on the RMS voltage of the Q node. as shown in Fig. 5(c). Thus, the T5 transistor with a V_{th} of −2.9 V is completely turned off. Hence, the QB node voltage of the proposed gate driver does not have a severe voltage drop. Fig. 7 shows the results of previously published paper [11] and the proposed circuit for normalized power consumption as V_{th}. Since the reported circuit [11] is different from the proposed circuit in terms of transistor model parameters, transistor sizes, resolution, gate line load, and driving voltages, each circuit has

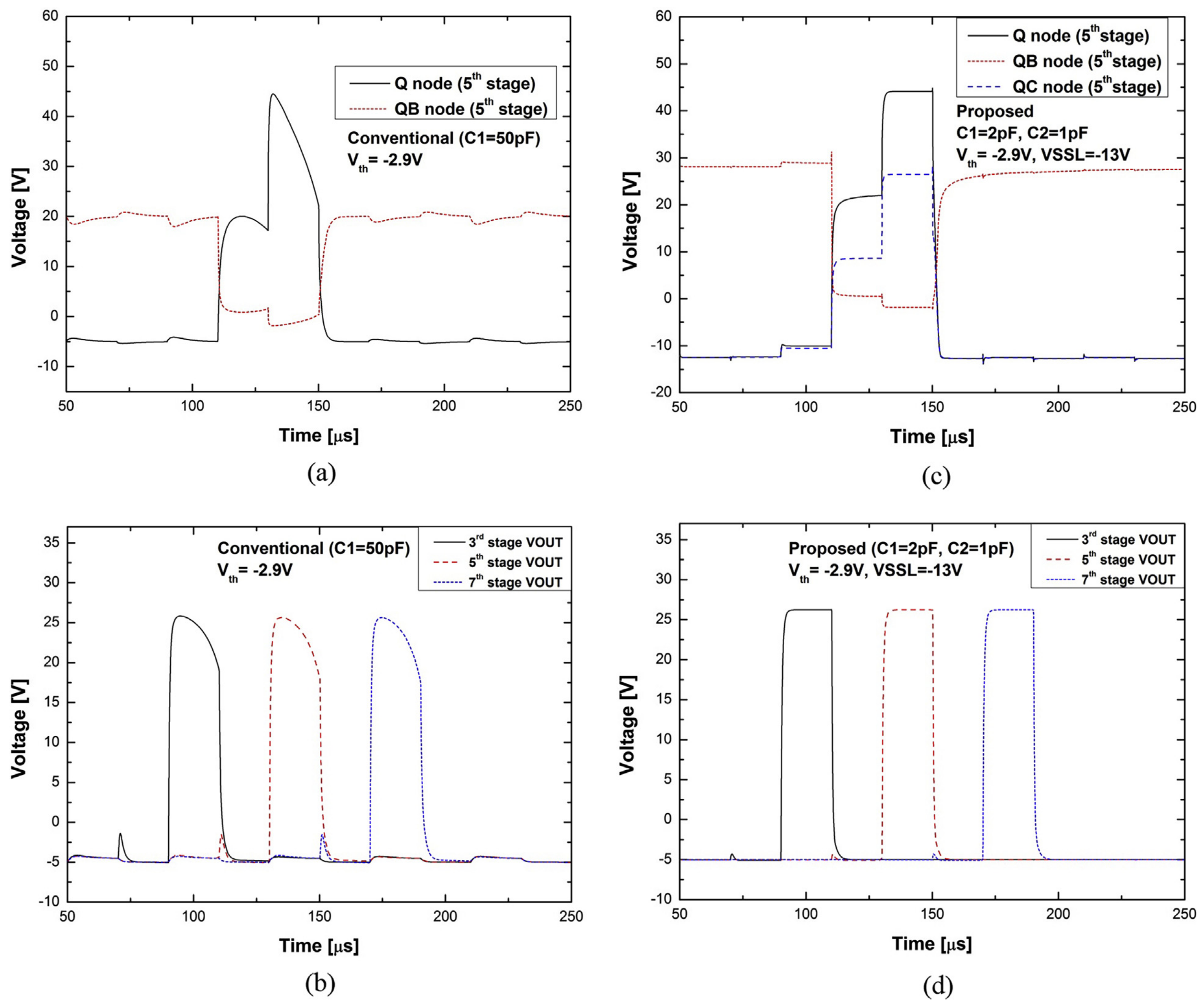
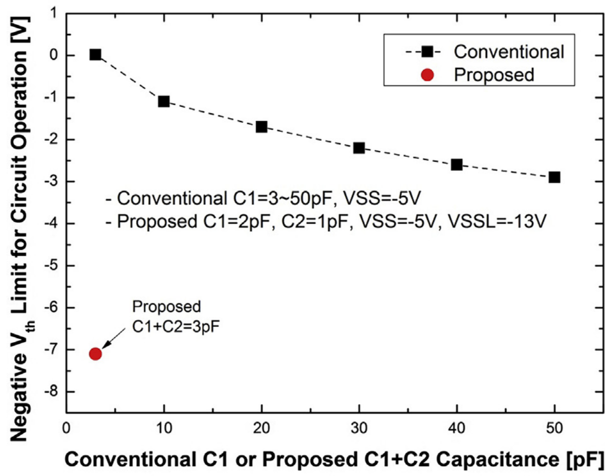


Fig. 5. The simulated voltage waveforms(V_{th} = −2.9 V): (a) conventional circuit Q and QB for 5th stage, (b) conventional circuit 3rd, 5th, and 7th stage VOUT, (c) proposed circuit Q, QB, and QC for 5th stage, and (d) proposed circuit 3rd, 5th, and 7th stage VOUT.

different power consumption in 3 V of V_{th}. The proposed circuit has a much higher value than the results of [11]. Therefore, the power consumption comparison of the circuits is not possible. On the other hand, it is possible to compare normalized power consumption as a function of V_{th}. In order to compare the power consumption for the negative V_{th} range, we normalized the data based on the value of V_{th} = 3 V [11]. The results of the proposed circuit maintain a very low normalized value when compared to the results of circuits in the published papers [15–16]. And it shows a similar value to the result of circuit in the published paper [11]. The power consumption of the proposed circuit with T7 TFT V_{gs} of 0 V at V_{th} of −5 V can maintain within 8.8 times that at V_{th} of 3 V. However, the power consumptions of the circuits in the published papers [15–16] with T5 TFT V_{gs} of 0 V at V_{th} of −5 V was 36.7–69.0 times that at V_{th} of 3 V. Fig. 8 shows the simulated voltage waveforms of the proposed circuit with V_{th} of −6.7 V. The QB node voltage of the proposed circuit with V_{th} = −6.7 V severely drops to the RMS of 19.8 V, as shown in Fig. 8(a). This is because the V_{gs} of T5 transistor is approximately equal to the RMS value of −4.92 V, and T5 transistor with V_{th} of −6.7 V is not completely turned off. The Q node and VOUT peak voltage of proposed circuit with V_{th} of −6.7 V drops when compared to V_{th} of 0.5 V, as shown in Fig. 8(b).

4. Conclusion

In this paper, we have presented a gate driver using depletion mode a-IGZO TFT with an improved negative V_{th} limit for circuit operation and low-power consumption. In the conventional gate driver circuits, due to depletion mode a-IGZO TFTs, the circuit transistors are not completely turned off. Thus, the voltage of the Q node of the conventional gate driver severely drops during the output pulse duration. To resolve that problem, we propose a new gate driver circuit. The proposed gate driver circuit can prevent Q node, the gate node of pull-up TFT, from discharging during the output pulse duration. For that purpose, our circuit applies sufficient negative V_{gs} to the switch TFTs connected to the Q node during that time. Consequently, the leakage current through them is suppressed even though they have a negative V_{th}. The proposed circuit has eleven transistors and two capacitors and it requires only two clock signals, which enables us to adopt the circuit at minimum extra cost. It works properly even when V_{th} is as low as −7.1 V. The normalized power consumption of the proposed circuit is also lowered compared with the previously reported circuits when the transistor has negative V_{th}. The power consumption of the proposed circuit for V_{th} of −5 V increases only nine times that for V_{th} of 3 V.



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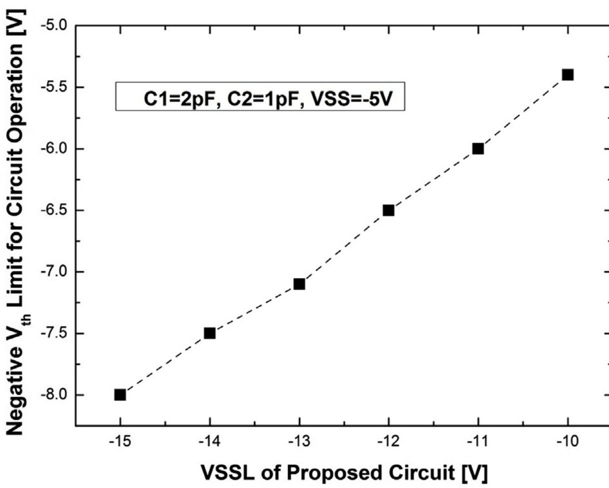

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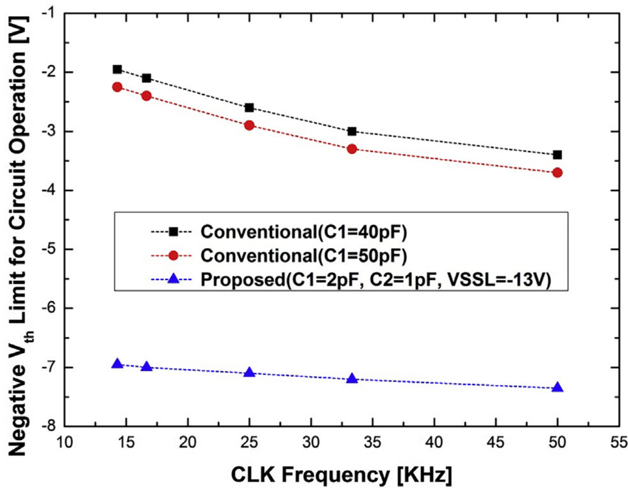


(c)

Fig. 6. The simulation results for negative V_{th} limit for circuit operation: (a) as conventional circuit C1 or proposed circuit C1 + C2, (b) as proposed circuit VSSL, and (c) as CLK frequency of conventional and proposed circuit.

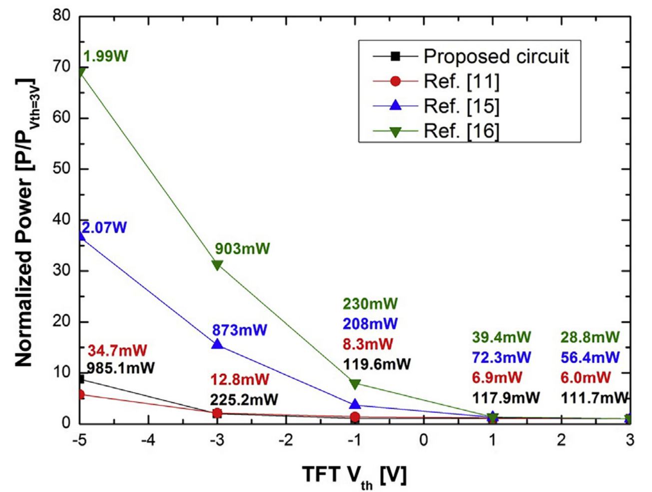
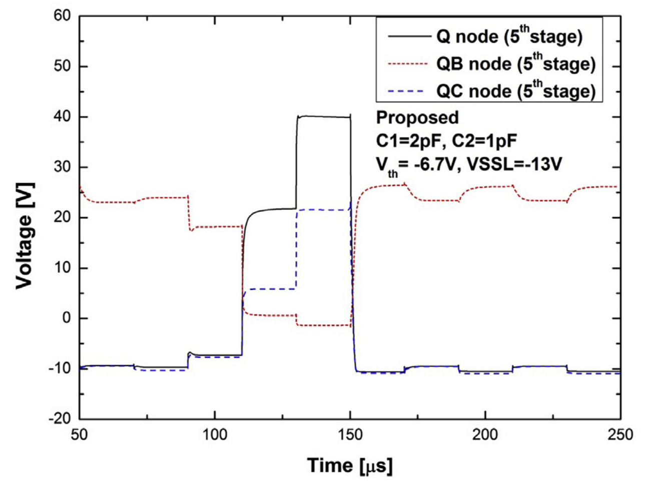


Fig. 7. The simulation results of normalized power consumption as a function of V_{th} for the proposed circuit and previously published paper [11]. (Proposed circuit: HD 768 lines panel, frame rate of 60 Hz, gate line load of 4 kΩ and 100 pF, −5 V to 28 V of CLK, −5 V of VSS, and −10 V of VSSL and [11]: VGA 480 lines panel, frame rate of 60 Hz, gate line load of 5 kΩ and 50 pF, 0–20 V of CLK, 0 V of VSS, and −5 V of VSSL).



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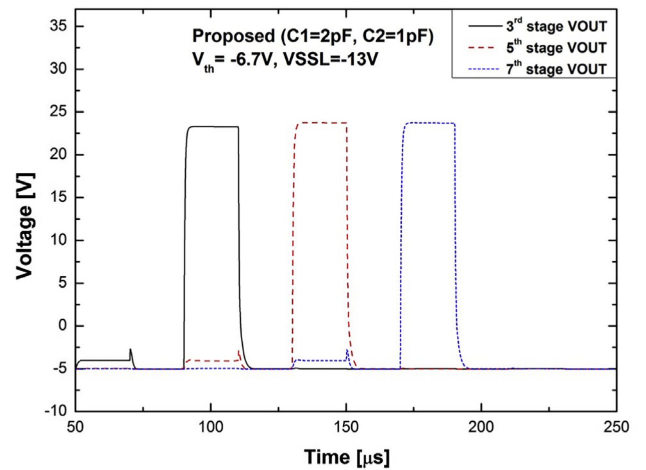

(b)

Fig. 8. The simulated voltage waveforms (V_{th} = −6.7 V): (a) proposed circuit Q, QB, and QC for 5th stage and (b) proposed circuit 3rd, 5th, and 7th stage VOUT.

Conflict of interest

There are no conflicts of interest to declare.

Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.displa.2018.03.003.

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