Non-volatile organic memory based on CdSe nano-particle/PMMA blend as a tunneling layer

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ABSTRACT

The use of nano-particle/polymer blend as the tunneling layer for non-volatile organic memory is an alternative to change and improve the device characteristics and performances. A non-volatile organic memory based on the pentacene semiconductor/poly(methylmethacrylate) (PMMA) + CdSe nano-particle blend tunneling insulator/PMMA gate insulator, is demonstrated by a simple fabrication process. We have observed the charging and discharging effect of CdSe NPs, using capacitance–voltage and current–voltage measurement. The capacitance and current change were observed by a charge transport between the pentacene semiconductor and the CdSe nano-particles. In addition, good reliability was confirmed by the retention characteristics.

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1. Introduction

Organic electronics have been studied with much interest over the last decade, due to their attractive features such as low cost, low temperature processing and mechanical flexibility [1–3]. Many applications such as organic solar cell [4], organic thin film transistor [5], organic circuit [6], organic light emitting diode [7], and organic sensor [8] are the focus of intense study. Recently, much attention is paid to nano-particles (NPs) floating gate organic memory devices as a promising candidate for the future non-volatile memory because of low power consumption, small device size, excellent stress leakage current induced (SILC) immunity and better retention from NPs-incorporated memory structures [9,10].

The tunneling insulator of the NPs floating gate memory is very important because it strongly affects the memory performance. In general, the inorganic insulator having good insulating properties is mostly used [11,12]. The use of inorganic insulators has several major drawbacks such as requiring relatively high temperature and complex fabrication process. In particular, the high-temperature processes for inorganic insulator is detrimental to organic memory device. For this reason, the proper organic insulator and low-temperature fabrication processes should be employed for the realization of NPs floating gate organic memory device. As an organic insulator, poly(methylmethacrylate) (PMMA) has been investigated because of its high resistivity, no hysteresis, thermal stability, and easy fabrication at low temperature [13,14]. Recently, Kim et al. [15] investigated the non-volatile nano-floating gate memory devices with pentacene organic semiconductor and PMMA tunneling insulator. They fabricated high performance organic field effect transistor having non-volatile memory characteristics using controlled gold NPs/polyelectrolyte composite layer and PMMA insulating layer.

In this study, we realized the NPs floating gate memory with CdSe NPs dispersed in PMMA insulating layer. The unique feature of this study is that the multilayers of CdSe NPs are formed inside the PMMA tunneling insulator, which provides a large memory window, potential multilevel charging characteristics, and improved retention properties. The NPs multilayers could be easily fabricated by simple spin-coating process of blended solution of CdSe NPs in PMMA.

2. Experimental

The devices in this study were fabricated with the process illustrated in Fig. 1. The metal–insulator–semiconductor (MIS) structure and top-contact pentacene thin film transistors (TFTs) were fabricated on the indium tin oxide (ITO) glass substrate. The ITO layer was used as gate electrode. As a control device without CdSe NPs,
PMMA (molecular weight 950 K, diluted in 4% anisole) as a gate insulator, was spin-coated twice at 4500 rpm for 60 s over ITO and subsequently baked at 160 °C for 30 min in a conventional oven. In this way, the thickness of PMMA layer was about 400 nm. For the NPs floating gate memory, the CdSe NPs solution (30 wt%) was mixed with PMMA solution. The CdSe NPs/PMMA layer was spin-coated on PMMA layer (200 nm) and subsequently baked at 160 °C for 30 min in a conventional oven to make PMMA gate insulator having homogeneously distributed CdSe NPs inside PMMA.

Fig. 2 shows the cross-sectional scanning transmission electron microscopy (STEM) image of CdSe NPs in PMMA layer. The CdSe NPs with a diameter of approximately 5 nm, coated with a thin ZnS layer and trioctylphosphineoxide (TOPO) as a surfactant, were used as purchased from Nanosquare Inc. The CdSe NPs had a composition of Cd:Se = 6:4, and the over-coating ZnS layer had a composition of Zn:S = 7:3. The CdSe NPs were dispersed in octane with a concentration of an order of 10^16/mL. The pentacene layer was deposited by thermal evaporation at a rate of 0.1 A/s to a thickness of about 70 nm at a high vacuum of <5 × 10^{-6} Torr. In MIS structure, a top metal electrode of Au was subsequently deposited by thermal evaporation through a shadow mask of 500 μm diameter size. In pentacene TFTs, the source and drain electrodes, a 100 nm thick Au layer were deposited through the shadow mask by thermal evaporation. The pentacene TFTs obtained thereby had a channel length (L) and width (W) of 100 μm and 1000 μm respectively. The electrical properties of devices were analyzed by capacitance–voltage (C–V) and current–voltage (I–V) characteristics at room temperature in ambient air using Agilent 4284A and Keithley 236 meter at a frequency of 100 kHz.

3. Results and discussion

C–V and I–V analysis of a control device without CdSe NPs did not show the hysteresis when the gate voltage (VGS) was swept from positive to negative and then back to positive voltage. Also, control devices did not show any capacitance shift (ΔC) and threshold-voltage shift (∆VTH) when the gate stress voltage of −40 V was applied for 2 s (Fig. 3). It indicated the density of charge trapping sites inside PMMA layer, while the PMMA–PMMA interface was negligible.

On the other hand, a hysteresis loops in counterclockwise direction were clearly observed in the memory device with CdSe NPs when the VGS was swept from +10 to −10 V, and then back to +10 V (Fig. 4a). Then, the sweeping VGS was increased up to ±40 V. Compared to the hysteresis in the range of ±40 V, the C–V curve shifted to negative direction, which means that CdSe NPs are positively charged, when the negative VGS is applied. The negative shift dur-
The application of negative $V_{GS}$ indicates that holes are transported from a pentacene layer to CdSe NPs or electrons are withdrawn from CdSe NPs. The shift of $C-V$ curve, representing memory window, increased as increasing the $V_{GS}$ sweep, by the increased charge injection. It should be noted that no shift was observed when the $V_{GS}$ was swept from positive to negative direction. It means that the positive charging of CdSe NPs can be achieved more efficiently than its negative charging on this device. Also, in $I-V$ analysis, a hysteresis loop in counterclockwise direction was clearly observed in the memory device with CdSe NPs when the $V_{GS}$ was swept from +10 to −20 V, and then back to +10 V (Fig. 4b).

Fig. 4 demonstrates the shift in $C-V$ and $I-V$ curve as a function of the amplitude of applied positive or negative gate voltage stress. The $C-V$ curve shifted to negative direction when $V_{GS}$ of −30, −40, −50 and −60 V were applied for 2 s. On the other hand, it slightly shifted towards positive direction after erasing the memory by a $V_{GS}$ of 60 V for 2 s. The memory window ($\Delta V$) after applying $V_{GS}$ was measured at a capacitance of 13.0 pF. The $\Delta V$ was 3, 4.5, 8 and 15 V at $V_{GS}$ of −30, −40, −50 and −60 V, respectively. Upon applying negative $V_{GS}$, the negative $\Delta V$ was attributed to the positive charging of CdSe NPs, and the positive charge in CdSe NPs were rejected by applying positive $V_{GS}$, whose characteristics were identical to the $C-V$ sweep results shown in Fig. 4. These charging and discharging effects of the CdSe NPs were observed in the pentacene TFTs structure. The $I-V$ curve shifted to negative direction when $V_{GS}$ of −30 and −40 V was applied for 2 s. On the other hand, it slightly shifted towards positive direction after erasing the memory by a $V_{GS}$ of 50 V for 2 s. The $\Delta V_{TH}$ was 2.33, and 5.18 V at $V_{GS}$ of −30 and −40, respectively. The shifted transfer curve returned to its initial position when a positive gate bias of $V_{GS}$ = 50 V was applied for 2 s.

The charge density ($Q$) in CdSe NPs can be estimated from equation:

$$Q = C \Delta V$$  \hspace{1cm} (1)

where $C$ is the capacitance between gate and the CdSe NPs [16]. Since PMMA layer with CdSe NPs was deposited by spin-coating from a uniform mixture of CdSe NPs and PMMA, it was considered that CdSe NPs were uniformly distributed in the PMMA layer (Fig. 2). While, the charge density was calculated by assuming that all the CdSe NPs were in the midst of PMMA layer. The amount of stored charges, $Q$, can thus be calculated from Eq. (1) as $3.13 \times 10^{-10}$, $1.67 \times 10^{-10}$, $9.39 \times 10^{-11}$, and $6.26 \times 10^{-11}$ C at the $V_{GS}$ of −60, −50, −40, and −30 V, respectively.

The charge retention characteristics of the devices were measured as a function of $\Delta C$ from the time-dependent capacitance change after programming with $V_{GS}$ of −50 V for 2 s. The $\Delta C$ was then measured at $V_{GS}$ = 0 V by sweeping gate voltage from 10 to −10 V in order to minimize the read disturbance. Because the voltage sweep range for read was too small to get the accumulation state of device, the charge retention was monitored by $\Delta C$. The charge retention at room temperature is shown in Fig. 6. The initial capacitance was 13.1204 pF, which increased to 13.2157 pF after 10$^4$ s, which corresponds to the charge retention of 83.34% as observed after 10$^4$ s, confirming that the proposed device had the potential to be considered for non-volatile memory applications.
4. Conclusion

We demonstrated a CdSe NPs/polymer blend as the tunneling layer for non-volatile organic memory. The charging and discharging in the CdSe NPs were observed in the C–V and I–V analysis of pentacene TFTs structure, showing the sufficiently large memory window and retention characteristics. Capacitance and $V_{TH}$ shift were observed as a function of increasing applied positive or negative gate voltage stress, indicative of successive charging and discharging of the CdSe NPs by hole injection. This study verified the feasibility of NPs floating gate organic memory device for the application to flexible organic devices.

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References