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Deposition of SiO_2 by Plasma Enhanced Chemical Vapor Deposition as the Diffusion Barrier to Polymer Substrates

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SiO_2 thin films were deposited at the temperatures $< 150°C$ by plasma enhanced chemical vapor deposition (PECVD) using a tetraethylorthosilicate (TEOS)/N_2/O_2 gas mixture, and the physical and chemical characteristics as well as the characteristics as a transparent diffusion barrier to H_2O were investigated. Using a gas combination of TEOS(40 sccm)/O_2(500 sccm)/N_2(100 sccm) at source power of 500 W and dc bias voltage of -350 V, SiO_2 with a stoichometric composition of SiO_2 and a smooth surface similar to the substrate could be deposited. When a multilayer diffusion barrier composed of parylene(800 nm)/SiO_2(100 nm)/parylene(800 nm)/SiO_2(100 nm)/parylene(800 nm) was formed on a polyethersulfone (PES) substrate, the water vapor transmission rate (WVTR) of the substrate was decreased from 54.1 to 0.3 gm/(m^2·day). [DOI: 10.1143/JJAP.44.1022]

KEYWORDS: SiO_2, parylene, polymer substrate, PECVD, low temperature

1. Introduction

The coating of diffusion barrier materials on polymer films has been studied extensively by food, pharmaceutical, and beverage packaging industries.[1–3] These diffusion barrier materials have been investigated intensively for the passivation of the next generation flat panel display (FPD) devices such as the organic thin film transistors (OTFTs) and organic light emitting diodes (OLEDs).[4–8] In particular, the use of flexible polymer substrates instead of sodalime glass substrates for the next generation FPD in order to reduce the weight, thickness, and cost of large area FPD requires a study of the transparent diffusion barriers to the polymer substrates. It is necessary not only to prevent water and oxygen from penetrating the polymer substrate so as not to degrade the devices but also to transmit visible light from the devices.

As the transparent diffusion barrier materials, various metal and semiconductor oxides have been investigated, and SiO_2 is one of the more widely examined materials as a diffusion barrier in addition to the dielectric materials in solid-state electronics.[9,10] Sputter deposition, evaporation, chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), etc. have been used to deposit these diffusion barrier materials.[1–3,8–11] Among these deposition methods, PECVD is one of the methods that can be used to deposit materials at a low temperature, with good step coverage and a high deposition rate.[11–13]

In this study, SiO_2 thin films were deposited by PECVD at temperatures $< 150°C$ using various source powers and dc bias voltages, and their physical and chemical characteristics were investigated for possible applications as diffusion barriers to polymer substrates. As a precursor, tetraethylorthosilicate (TEOS) was used because of its lower probability of particulate formation and a higher chemical stability and safety in handling compared with other silicon sources such as SiH_4.[12,13] In addition, its water vapor transmission rate (WVTR) was measured by forming a multilayer composed of parylene/SiO_2/parylene/SiO_2/parylene on the polymer substrates.

2. Experimental

The PECVD system used to deposit the SiO_2 is shown in Fig. 1. As shown in the figure, the plasma source was a conventional planar inductively coupled plasma (ICP) source with a 3.5 turn copper spiral coil on the top of the chamber to generate the ICP plasmas by applying 100–900 W 13.56 MHz rf power. The substrate holder was 4 inches in diameter and was biased from -150 to -450 V using a separate 13.56 MHz rf power supply whilst maintaining a substrate temperature $< 150°C$ to provide ion bombardment during SiO_2 film growth. A mixture of the precursor and dilution gases composed of TEOS carried by 40 sccm N_2, 100 sccm of N_2, and 500 sccm O_2 was fed to the chamber through a gas ring located in the top-edge of chamber. TEOS was heated to 40°C using a circulation bath and the gas line to the chamber was maintained at 80°C using a heating band.

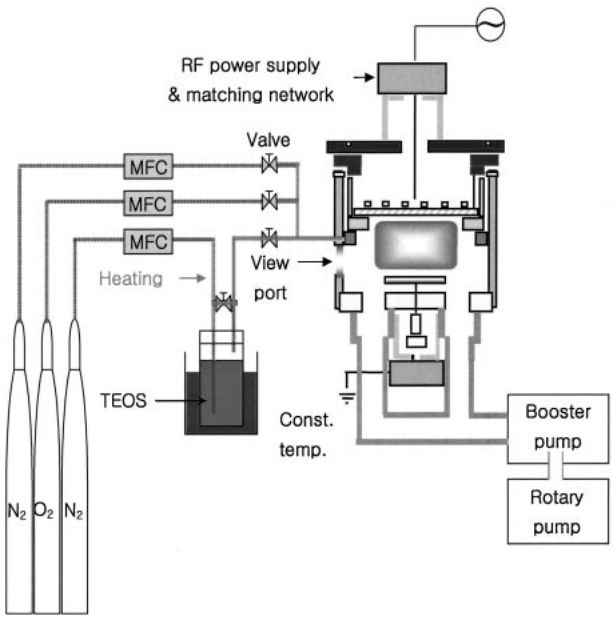


Fig. 1. Schematic diagram of the SiO_2 PECVD system used in the experiment.

The SiO_2 thin films were deposited on the substrates such as silicon wafer, sodalime glass, and PES. Even though the substrate holder temperature was maintained at room temperature using a chiller, the temperature of the substrates such as PES and sodalime glass increased during the growth using the high dc bias voltages due to the low thermal conductance. The temperature of the substrate during the growth of SiO_2 was measured using a Luxtron temperature probe (Luxtron Inc., 712 fluoroptic thermometer) attached on the top of the substrates. The thickness and roughness of the grown SiO_2 was measured using a step profilometer (Tencor Inc., Alpha step-500) and an atomic force microscope (AFM) (Thermo-Microscopes Inc., CP Research), respectively. The surface roughness was also observed using field emission scanning electron microscopy (FESEM, Hitachi Ltd., S-4700). X-ray photoelectron spectroscopy (XPS, VG Microtech Inc., ESCA2000) was used to examine the composition of the deposited SiO_2.

For the measurement of the WVTR, SiO_2 was deposited alternatively with parylene on the PES substrates to form a multilayer diffusion barrier. The parylene was deposited using a parylene coater (SCS Inc., PDS 2010 LABCOTER) at 20–40 mTorr with a thickness ranging from 800 to 300 nm. The details of the parylene coating system are reported elsewhere.[14] The optical transmittances of the deposited SiO_2 and parylene were measured using a UV spectrometer (Scinco Inc., UV S-2100). A WVTR measurement system (MOCON Inc., PERMATRAN-W model 3/33) was used to measure the H_2O transmission rate of the multilayer diffusion barrier on the PES substrate.

3. Results and Discussion

Figure 2 shows the effect of the source power and dc bias voltage on the SiO_2 deposition rate for the gas combination of 40 sccm TEOS by a N_2 flow, 500 sccm of O_2, and 100 sccm of N_2. When the source power and the dc bias voltage were varied separately, the dc bias voltage and the source power were maintained at 500 W and −350 V, respectively. As shown in the figure, the increase in the source power from 100 to 900 W decreased the SiO_2 deposition rate until 700 W had been reached and a further increase in the source power appeared to saturate the deposition rate. When the source power was 100 W, the deposition rate was the highest at 53 nm/min. However, the deposited film was very soft so that it was easily scratched by tweezers. As the source power was increased, the hardness of the films was increased. When the bonding states of the SiO_2 deposited at low source powers were investigated by a Fourier transform infrared spectroscopy, $Si–(CH)_3$ bonds were observed. (data not shown) Therefore, the higher deposition rate at the lower source power appears to be related to the adsorption of non- or partially dissociated TEOS rather than to the deposition of stoichiometric SiO_2. By increasing the source power, the TEOS was decomposed further to form SiO_2 on the substrate, and at a source power > 700 W, the dissociation of TEOS appears to be complete.

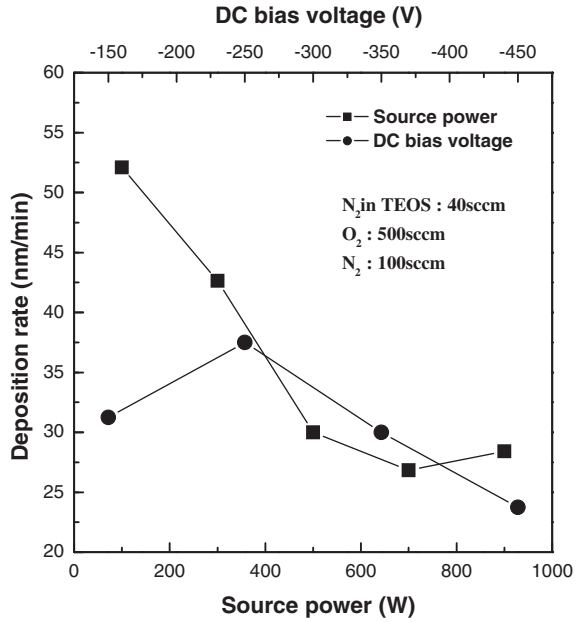


Fig. 2. Deposition rate of the SiO_2 films by PECVD at low temperatures as a function of the source power and dc bias voltage. (condition: N_2 in TEOS 40 sccm, O_2 flow rate 500 sccm, and N_2 flow rate 100 sccm)

Figure 2 also shows the effect of the dc bias voltage on the deposition rate of SiO_2 at a 500 W source power. As shown in the figure, the SiO_2 deposition rate showed a maximum at a dc bias voltage −250 V and a further increase in the dc bias voltage decreased the deposition rate. The initial increase in the SiO_2 deposition rate with increasing dc bias voltage appears related to the increased dissociation of TEOS adsorbed on the substrate to form SiO_2. However, as the dc bias voltage was further increased, the sputter etching rate of SiO_2 was also increased resulting in a lower overall SiO_2 deposition rate. The increase in the dc bias voltage also increased the density of the SiO_2. Therefore, the hardness of the SiO_2 was increased with increasing dc bias voltage. When the substrate temperature was measured on the PES substrates using a Luxtron temperature probe, the substrate temperature was increased with the increase in the dc bias voltage and the substrate temperature $> 180°C$ were obtained during deposition when both the source power and the dc bias voltage were higher than 700 W and −350 V. Therefore, in order to prevent deformation of the PES substrate during deposition, the dc bias voltage needs to be kept less than or equal to −350 V.

Table I shows the composition of the deposited SiO_2 measured by XPS for the various source powers at a dc bias voltage of −350 V and for various bias voltages at source power of 500 W. As a reference, the composition of the SiO_2

Table I. Atomic percentages of SiO_2 films measured by XPS for different source power (−350 V of dc bias voltage) and for different dc bias voltage (500 W of source power). As a reference, the atomic percentages of SiO_2 deposited by a commercial CVD was included.

Method of SiO_2 deposition		Chemical composition		
		Si 2p (%)	C 1s (%)	O 1s (%)
Thermal CVD		38.3	0.4	61.3
DC bias voltage −350 V	300 W	37.6	0.4	62.0
	500 W	37.7	0.3	62.0
	900 W	37.7	0.3	62.0
Source power 500 W	−150 V	37.4	1.1	61.5
	−250 V	38.1	0.2	61.7
	−350 V	37.7	0.3	62.0

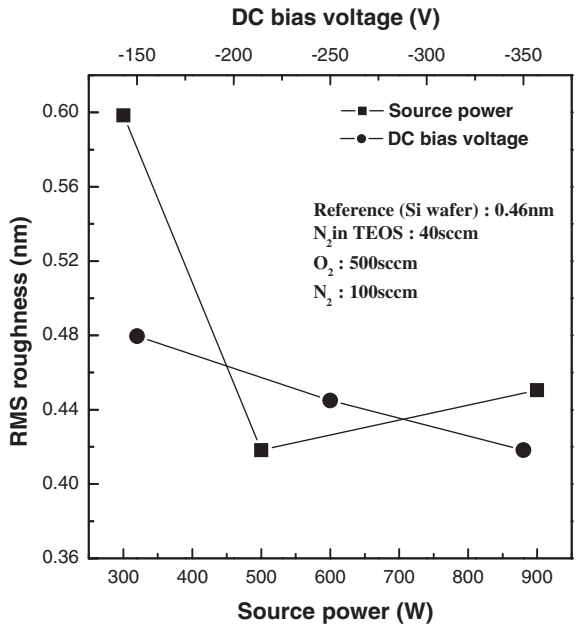
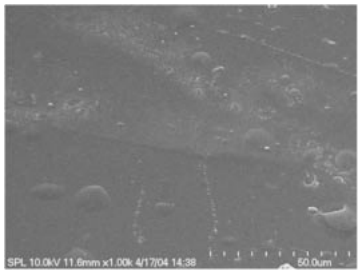
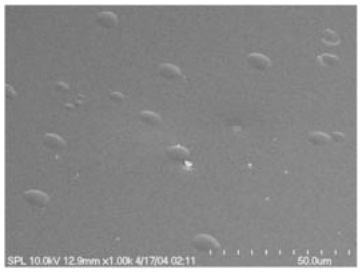


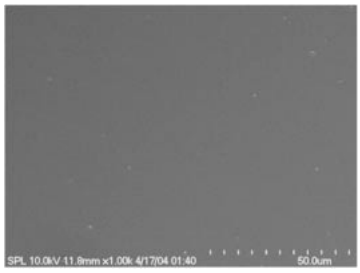
Fig. 3. RMS roughness of the SiO_2 films deposited on a silicon wafer (the roughness is 0.459 nm) as a function of the source power and dc bias voltage measured by AFM. (condition: N_2 in TEOS 40 sccm, O_2 flow rate 500 sccm, and N_2 flow rate 100 sccm)



(a) Source power 300W, dc bias voltage –350V



(b) Source power 500W, dc bias voltage –150V



(c) Source power 500W, dc bias voltage –350V

Fig. 4. Surface morphology of the deposited SiO_2 films as a function of the source power and dc bias voltage observed by FESEM. (condition: N_2 in TEOS 40 sccm, O_2 flow rate 500 sccm, and N_2 flow rate 100 sccm)

deposited by a commercial CVD was also measured. As shown in the Table, most of the deposited SiO_2 had a similar composition to that produced by thermal CVD except for the SiO_2 deposited at the low dc bias voltage of -150 V. When the dc bias voltage was low, a higher carbon percentage was obtained possibly due to the adsorption of non-dissociated TEOS. Therefore, it is believed that a stoichiometric SiO_2 film can be deposited on the polymer substrates by a PECVD with a 500 W source power and a -350 V dc bias voltage using TEOS(40 sccm N_2)/N_2(100 sccm)/O_2(500 sccm) at the temperature $< 150^{\circ}$C.

100 nm thick SiO_2 thin films were deposited on silicon wafers at various dc bias voltages (at 500 W of source power) and various source powers (at -350 V of dc bias voltage), and the surface roughness of the deposited SiO_2 films were measured by AFM (Fig. 3). As shown in the figure, the increase in the source power decreased the surface roughness, and when the source power was > 500 W, the surface roughness was similar to that of the silicon surface (0.458 nm). The high surface roughness at the low source powers appears to be related to the adsorption of non-dissociated TEOS on the substrate. The increase in the dc bias voltage also decreased the surface roughness as a result of the increased dissociation of the adsorbed TEOS and the densification of the deposited SiO_2. The effect of the adsorption of non-dissociated TEOS on the deposited SiO_2 at the low source powers and low dc bias voltages could be observed by FE-SEM as shown in Fig. 4. As shown in the micrographs, when the source power was 300 W and the bias voltage was -150 V, the surface of the deposited SiO_2 exhibited bubble-like areas possibly related to the incorporation of non-dissociated TEOS in the film. However, when the source power was > 500 W and the dc bias voltage was less than -350 V, the surface was smooth and no such bubbles could be observed.

In order to apply the above optimized SiO_2 as the diffusion barrier materials to the polymer substrates or to the devices, organic material layers are generally used in addition to the inorganic diffusion barrier materials in order to planarize the substrate surface before depositing the SiO_2 and to release the stress of the deposited SiO_2. In these experiments, parylene was deposited as the organic material on the sodalime glasses using a commercial parylene coater at room temperature at various pressures, and its roughness was examined using AFM as a function of the operational pressure and the thickness of parylene, and the results are shown in Fig. 5. The surface roughness of the deposited parylene increased with increasing the film thickness and with increasing operational pressure possibly due to the increased particle formation on the surface at the higher pressures and with time. For the investigated conditions, the lowest roughness of approximately 4.96 nm could be obtained at 20 mTorr and with a thickness of 800 nm while the roughness of the sodalime glass substrate was 3.11 nm.

In order to apply the diffusion barrier materials for the FPD substrates, the optical transmittance of the deposited materials needs to be high. Figure 6 shows the optical transmittances of the SiO_2 and parylene deposited on the

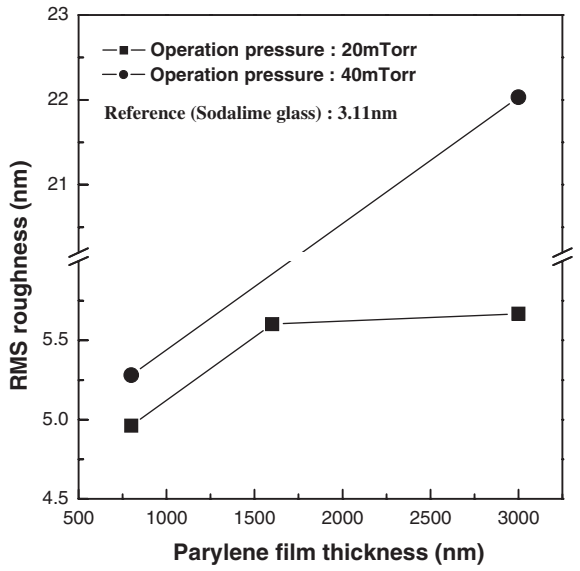


Fig. 5. RMS roughness of the parylene films deposited on a sodalime glass (the roughness of 3.11 nm) as a function of the deposition thickness and operation pressure measured by an AFM.

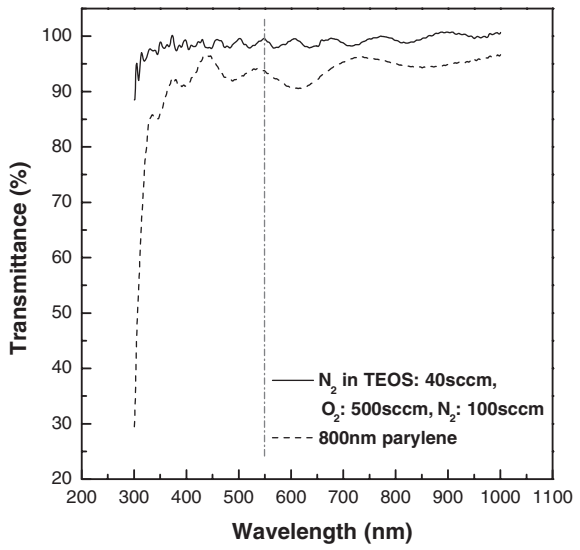


Fig. 6. Optical transmittance of the SiO_2 films deposited by PECVD on a sodalime glass substrate (condition: N_2 in TEOS 40 sccm, O_2 flow rate 500 sccm, N_2 flow rate 100 sccm, source power 500 W, and dc bias voltage −350 V) and the parylene films (800 nm, 20 mTorr) measured by a UV spectrometer. The vertical dash-dotted line indicates a wavelength of 550 nm, which was used as the wavelength for measuring the optical transmittance.

sodalime glass measured by a UV spectometer. The 100 nm thick SiO_2 was deposited at a 500 W source power and a −350 V dc bias voltage with TEOS(N_2 40 sccm)/O_2(500 sccm)/N_2(100 sccm) gas mixtures and the 800 nm thick parylene was deposited at 20 mTorr. As shown in the figure, the optical transmittances of the 100 nm thick SiO_2 and 800 nm thick parylene were >99% and 93% at 550 nm, respectively. Therefore, the deposited films showed sufficient transmittances for applications to the FPD substrates.

Using the optimized SiO_2 thin film and parylene, a multilayer diffusion barrier composed of parylene(800 nm)/SiO_2 (100 nm) / parylene (800 nm) / SiO_2 (100 nm) / parylene

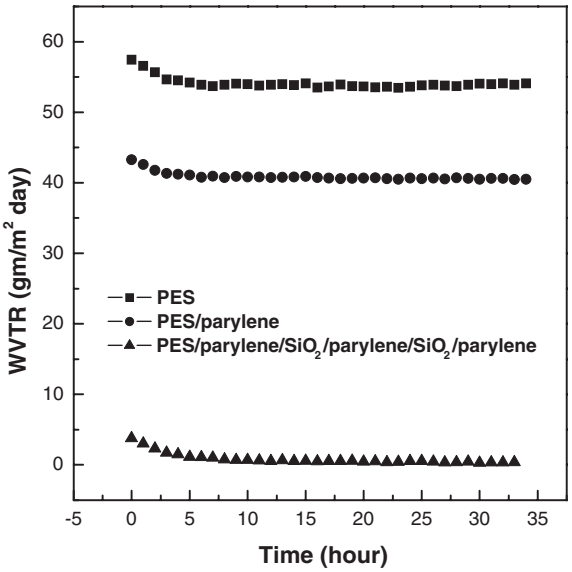


Fig. 7. WVTR of the 300 μm thick PES substrate, PES/parylene(800 nm), and PES/parylene(800 nm)/SiO_2(100 nm)/parylene(800 nm)/SiO_2(100 nm)/parylene(800 nm).

(800 nm) was deposited on the 300 μm thick PES substrate, and its WVTR was examined, and the result is shown in Fig. 7. The measurement environment was 100% humidity, 37.8 □, and 6.4 sccm N_2 flow rate. As a reference, the WVTR of the PES substrate itself and that of a 800 nm thick parylene on the PES substrate were also measured. As shown in the figure, the WVTR of the PES substrate was 54.10 gm/(m^2·day), that of 800 nm thick parylene on the PES substrate was 40.4 gm/(m^2·day), and that of the multilayer diffusion barrier composed of parylene(800 nm)/SiO_2 (100 nm) / parylene (800 nm) / SiO_2 (100 nm) / parylene (800 nm) on the PES substrate was 0.3 gm/(m^2·day). Therefore, by depositing a multilayer diffusion barrier on the PES substrate, a significant decrease in the WVTR could be obtained. However, the WVTR obtained in these experiments is not sufficient because the OLED and OTFT devices require a WVTR $> 10^{-6}$ gm/(m^2·day) and 10^{-2} gm/(m^2·day), respectively. It is believed that, the WVTR required for OLED and OTFT devices could be satisfied by the formation of a higher order multilayer diffusion barrier composed of SiO_2 and parylene.

4. Conclusion

In this study, SiO_2 was deposited at temperatures < 150°C by a PECVD using TEOS/N_2/O_2, and its physical and chemical characteristics were examined as a functions of the source power and dc bias voltage. In addition, its WVTR characteristics were investigated using a multilayer composed of parylene/SiO_2/parylene/SiO_2/parylene.

When the SiO_2 was deposited at low source powers and low dc bias voltages, the deposited SiO_2 showed a rough surface and a non-stoichiometric composition possibly related to the adsorption of non-dissociated TEOS on the substrate surface. In addition, the physical and chemical characteristics similar to the stoichiometric SiO_2 could be obtained with a smooth surface close to the substrate by increasing the source power and dc bias voltage. The substrate temperature was increased to > 180°C during

deposition as a result of the increase in the dc bias voltage less than -350 V at a source power > 700 W due to the low thermal conductance of the glass substrates and polymer substrates. Therefore, a dc bias voltage less than -350 V could not be applied to the polymer substrates. A transparent SiO_2 film with the stoichiometric composition and a surface roughness similar to the substrate could be obtained using a 500 W source power, a -350 V dc bias voltage, and a gas mixture of TEOS(N_2 40 sccm)/O_2(500 sccm)/N_2(100 sccm) at low temperature. When a multilayer diffusion barrier composed of parylene(800 nm)/SiO_2(100 nm)/parylene(800 nm)/SiO_2(100 nm)/parylene(800 nm) was deposited on the PES substrate with the optimized SiO_2, the WVTR decreased from 54.10 to 0.3 gm/(m^2·day). Even though the WVTR obtained is not low enough for OLED or OTFT devices, it is believed that, the WVTR required for OLED and OTFT devices could be satisfied by the formation of a higher order multilayer diffusion barrier composed of SiO_2 and parylene.

Acknowledgments

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