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To cite this article: Soo-Gang Kim *et al* 2020 *Nanotechnology* **31** 265302

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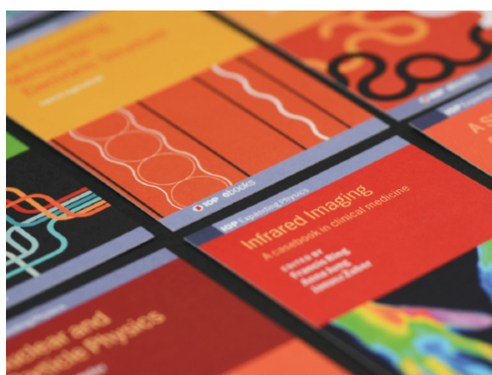
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Nanotechnology 31 (2020) 265302 (12pp) https://doi.org/10.1088/1361-6528/ab7c75

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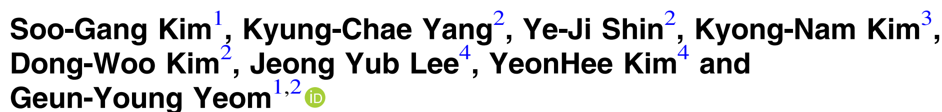

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Received 9 February 2020
Accepted for publication 4 March 2020
Published 13 April 2020

Abstract

The etch characteristics of Si and TiO_2 nanostructures for optical devices were investigated using pulse biased inductively coupled plasmas (ICP) with $SF_6/C_4F_8/Ar$ and BCl_3/Ar, respectively, and the results were compared with those etched using continuous wave (CW) biased ICP. By using pulse biasing compared to CW biasing in the etching of the line/pillar nanostructures with various aspect ratios, there was a reduction of the aspect ratio dependent etching (ARDE) and therefore, uniform etch depths for nanostructures with different pattern widths, as well as the improvement of the etch profiles without any notching, were obtained not only for silicon nanostructures but also for TiO_2 nanostructures. The investigation has determined that the improvement of etch profiles and reduced ARDE effect when using pulse biasing are related to the decreased surface charging caused by neutralization of the surface and the improved radical adsorption (or etch byproduct removal) on the etched surfaces during the pulse-off period for pulse biasing compared to CW biasing.

Keywords: pulsed PLASMA etching, Si nanostructure, TiO_2 nanostructure, etch profile, aspect ratio dependent etch (ARDE)

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon and titanium dioxide (TiO_2) based nanostructures variously arranged in the sub-wavelength scale have been widely investigated for optical devices based on nanophotonics [1–8]. These artificially designed nanostructures, named 'metamaterials', have unique optical properties which overcome former optical limitations, so they can have various optical applications with enhanced capability such as lenses [4], reflectors [5], polarizers [6], and light extractors [7]. For more than a decade, research on optical metamaterials were almost exclusively associated with metallic (i.e., plasmonic) materials [9–11]. However, metallic materials have a high extinction coefficient which leads to low optical efficiency by absorbing a wide spectrum of light. In contrast, nonmetallic materials such as silicon, silicon nitride, titanium dioxide, etc have very low absorption losses in the near infrared and visible wavelength range [1, 12–14], therefore, these days, more research is concentrated on the fabrication of various metamaterials composed of these materials.

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One of the main issues at present is the nanofabrication of the high quality and high aspect ratio nanostructures required for the above materials, the lack of which severely affects the optical properties [4, 15, 16]. The nanostructures of these materials can be fabricated using dry etching methods. Even though nanostructures have been fabricated using atomic layer deposition (ALD) on patterned photoresist templates, followed by the removal of the resist template, due to other problems such as the extremely long processing time, additional process steps, limitations on materials deposited by ALD, etc, dry etching methods are preferred as reliable manufacturable methods [1, 16–19]. Dry etching methods have been widely used for the production of semiconductor devices requiring anisotropic etch features as the size of devices can be decreased [20, 21]. However, in the dry etching of anisotropic nanoscale etch features with high aspect ratios, some problems such as charge accumulation induced notching [22–24], micro-trenching [25, 26], aspect ratio dependent etching (ARDE) [27, 28], etc still remain to be solved. In the nanostructure fabrication of optical metamaterials using dry etching, these problem not only make it hard to fabricate the desired nanostructures but also can affect their optical properties.

As one of the most effective etch techniques to overcome these problems, the pulsed plasma etching method, which adjusts plasma properties by turning the rf powers on and off has been investigated recently and intensively [29–31]. By choosing several kinds of pulsing techniques (source pulsing, bias pulsing, synchronous pulsing, asynchronous pulsing, etc) and controlling the pulse parameters (pulse frequency and duty ratio), pulse plasma etching offers extra process knobs which are not available in conventional dry etching, that is, etching using continuous wave (CW) rf powers. These pulse plasma techniques are known to offer the opportunity to control the ion energy distribution (IED), electron temperature, density of plasma species, dissociated radical species, etc, which can achieve desirable etch characteristics with high etch anisotropy, etch uniformity and relaxation of the charge related problems [29–36].

Until now, pulse plasma techniques have been mostly applied to semiconductor integrated circuit (IC) fabrication and no such pulsed plasma techniques have been investigated for the fabrication of other non silicon IC-based devices such as optical metamaterials, micro-electromechanical system (MEMS) devices, etc even though the reactive ion etching (RIE) lag effect was observed during the anisotropic etching of devices using CW plasmas [37]. Therefore, in this study, for the fabrication of optical metamaterials, silicon (Si) and titanium dioxide (TiO_2) nanostructures composed of nanograting (line) and nanopost (pillar) on glass substrates were formed using inductively coupled plasma (ICP) etching with $SF_6/C_4F_8/Ar$ and BCl_3/Ar, respectively. The effects of the pulse biased ICP etching on the plasma characteristics and etch characteristics of Si and TiO_2 was investigated and the results were compared with those generated from CW biased ICP etching. Also, a possible etch mechanism for the pulse biased etching was investigated.

2. Experimental details

For the etching of Si and TiO_2 nanostructures, a 200 mm ICP etch system (STS-PLC) was used and the schematic of the ICP etch system is shown in figure 1. For both the ICP source power and the substrate bias power, 13.56 MHz radio frequency power generators were used. For all etch experiments, the ICP source power was kept at 700 W while the substrate DC bias voltage was kept at −50 V for continuous wave (CW) bias power conditions by applying the rf power of 700 W. For the pulsed etch conditions, pulse bias power conditions with 1 kHz of pulse frequency and 50% of pulse duty ratio was used while supplying continuous rf power to the ICP source. During this pulse bias power condition, the average DC bias voltage during the power-on period was also maintained at −50 V. The substrate temperature was maintained by supplying 10 °C water to the substrate from a chiller by using 10 Torr He gas as a heat transfer gas between the wafer and substrate. The etch gases were injected from the top center of the chamber as shown in figure 1. For the Si nanostructure etching, a gas mixture composed of SF_6(10 sccm)/C_4F_8(34 sccm)/Ar(10 sccm) was used and for the TiO_2 nanostructure etching, a gas mixture composed of BCl_3(15 sccm)/Ar(45 sccm) was used. For all etch experiments, the process pressure was maintained at 7 mTorr. The etch samples, 600 nm (or 300 nm)-thick Si and 670 nm-thick TiO_2 deposited on glass wafers were used and the samples were patterned with 400 nm-thick photo-resist (PR) by KrF photolithography or 350 nm-thick E-beam resist (EBR) by electron beam lithography. The line (nanograting) and pillar (nanopost) patterns as shown in figure 2 with the same feature size and different pitch size for PR patterns (for the EBR pattern, with the different feature size and same pitch size) were used in this experiment to identify etch properties depending on the pitch size and the aspect ratio. The 600 nm thick Si and 670 nm thick TiO_2 on glass substrates which were line-patterned with the same feature size of 150 nm and different space width (different pitch size), and therefore, with the different aspect ratio (estimated by the pattern depth/pattern opening width) of 1∼2.8 were used for the etching. For Si, 300 nm thick Si on glass substrates line-patterned with 350 nm thick EBR having the aspect ratio of 2.0∼5.0 with the same pitch size of 420 nm was also used for the etching.

A field emission scanning electron microscope (FE-SEM; Hitach, S4700) was used to measure the etch depth (the etch rate was obtained by calculating the etch depth/etch time even though the instant etch rate can be varied as the etch depth is increased) and etch profile of the etched features. The etch selectivity was calculated by using the following equation; Etch selectivity of Si or TiO_2 = (Etch depth of Si or TiO_2)/(Thickness of PR or EBR before etching—Thickness of PR or EBR after etching). To understand the pulse bias etching, the instant voltages to the substrate during CW and pulse bias conditions were measured using a high voltage probe (Tektronix., P6015A). In addition, the ion energy to the substrate was measured using a retarding field analyzer (RFA; Impedans Ltd, SEMION) with four grids (G0(substrate potential): entrance grid, G1: ion/electron repelling grid, G2: analyzer

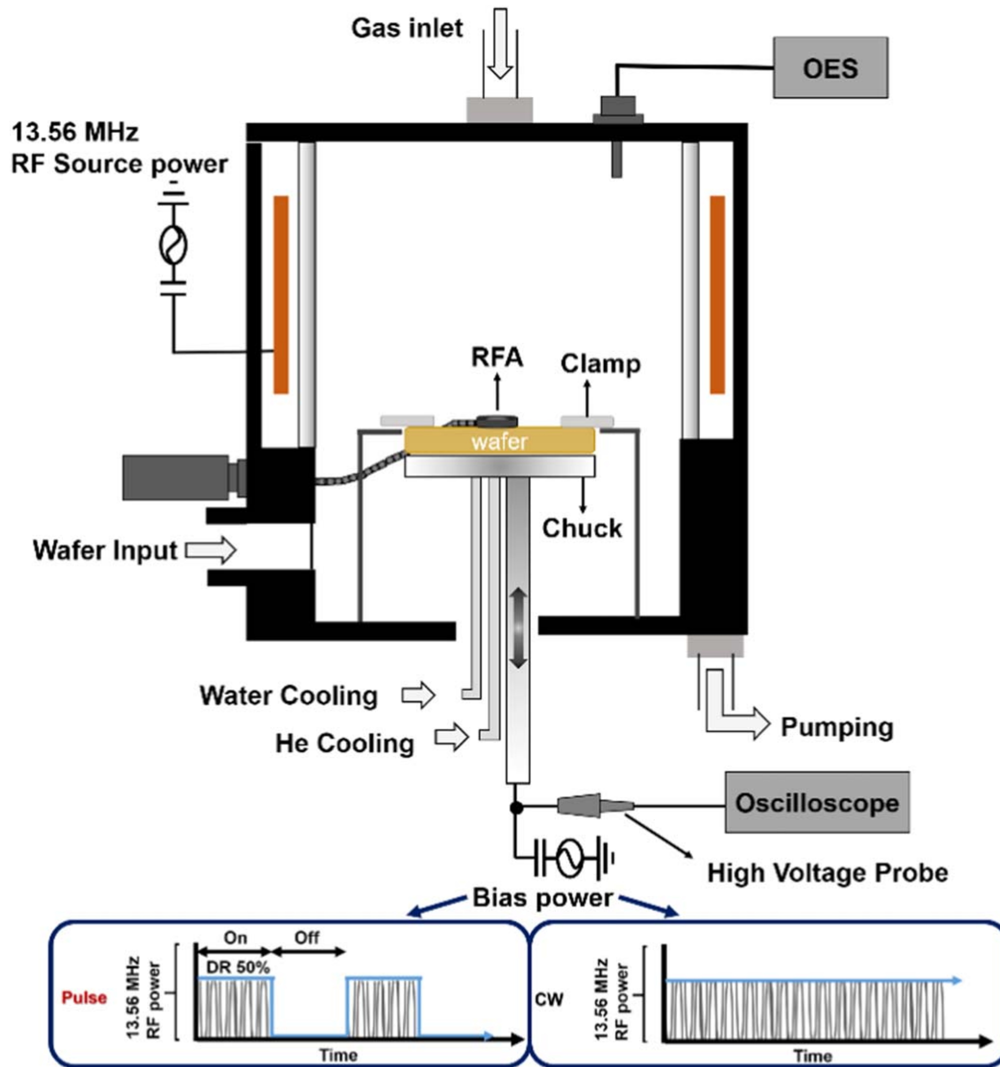

Figure 1. Schematic diagram of the pulse/CW biased ICP etching system.

grid, G3: secondary electron suppressing grid) and one collector (C: ion/electron collector) located on the biased (pulse bias or CW bias) substrate as shown in figure 1 to obtain the ion energy distribution function (IEDF) to the biased substrate. The voltages of the three grids in the RFA were varied to observe the ion energy distributions of positive ion and negative ion in the CW and pulsed bias conditions [38–41]. And the species of bulk plasma were compared in both the CW and pulse bias conditions using an optical emission spectrometer (OES; Andor, iStar734). In addition, the chemical compositions of the etched Si and TiO_2 were observed using x-ray photoelectron spectroscopy (XPS; VG Microtech Inc., ESCA2000).

3. Results and discussion

The normalized etch rates of Si and TiO_2 nanostructures (nanograting and nanopost) on glass substrates and their etch selectivities to PR (or EBR) in CW bias conditions (−50 V DC bias voltage) and pulse bias conditions (1 kHz of pulse frequency and 50% duty cycle; the average DC bias voltage during the pulse-on period was −50 V) were investigated. The results for the line pattern (nanograting) are shown in figures 3(a) and (b) for the etch rates and etch selectivities, respectively. The etch rates of blanket Si and TiO_2 without patterns were also measured and the etch rates of patterned Si and TiO_2 were normalized to the etch rates of blanket Si and TiO_2, respectively. For the Si etching, a gas mixture of SF_6 (10 sccm)/C_4F_8(34 sccm)/Ar(10 sccm) was used and, for TiO_2 etching, a gas mixture of BCl_3(15 sccm)/Ar(45 sccm) was used and, for all etch experiments, the process pressure and the ICP source power was maintained at 7 mTorr and 700 W, respectively. At the above conditions, the etch rates of blanket samples were $\sim$218 nm min^{-1} (CW) and $\sim$189 nm min^{-1} (Pulse) for Si with SF_6/C_4F_8/Ar and $\sim$43 nm min^{-1} (CW) and $\sim$41 nm min^{-1} (Pulse) for TiO_2 with BCl_3/Ar. Therefore, the etch rates for the pulse bias conditions were lower than those for CW bias conditions but the etch rates were higher than 50% for the 50% pulse bias condition. (the etch rates higher than 50% of CW condition with 50% pulse bias condition are believed to be related to the

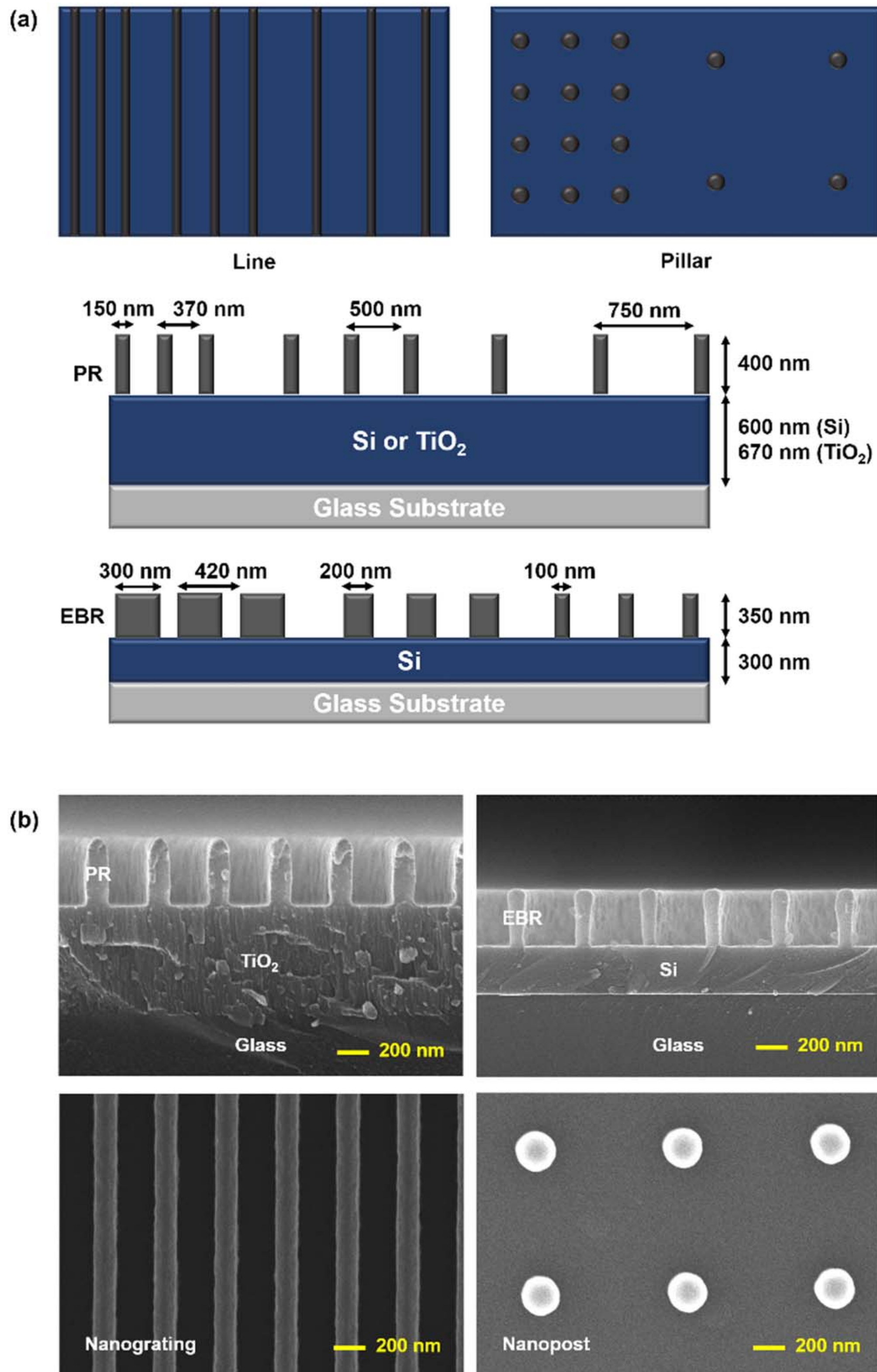

Figure 2. (a) Schematic drawing and (b) SEM images of the Si/TiO_2 samples with different line/pillar patterns used in this experiment.

removal of charging during the pulsed etching, therefore, higher ion enhanced chemical etching during pulse on-time by more ions arriving at the bottom of the etch features. But, the exact reason for higher etch rate for pulsing needs to be investigated further.)

As shown in figure 3(a), for TiO_2, for the aspect ratio of 1.0, the etch rate for the CW bias condition was a little lower than that of the blanket (aspect ratio = 0) TiO_2, and, as the aspect ratio was increased from 1.0 to 2.8, the normalized etch rate was decreased from 0.82 to 0.66. For Si, at the

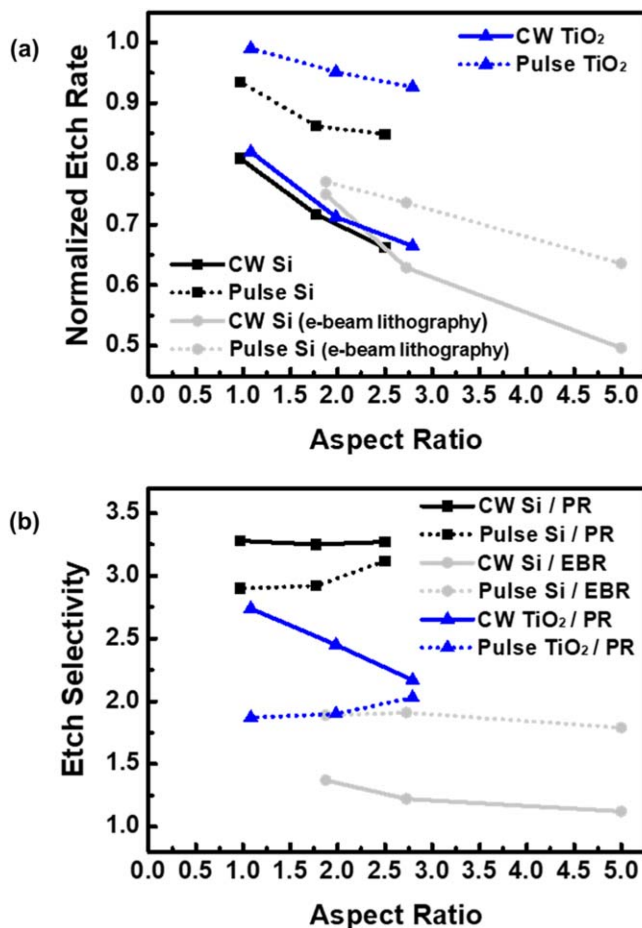

Figure 3. Normalized etch rates and etch selectivities of Si and TiO_2 lines (nanogratings) with different pattern widths for CW and pulsed bias conditions. For Si, a gas mixture of SF_6 (10 sccm)/C_4F_8(34 sccm)/Ar(10 sccm) was used and, for TiO_2, a gas mixture of BCl_3(15 sccm)/Ar(45 sccm) was used. The etch rates were normalized to the blanket sample etch rates. The etch rates of blanket samples: ~218 nm min^{-1} (CW) and ~189 nm min^{-1} (Pulse) for Si with SF_6/C_4F_8/Ar and ~43 nm min^{-1} (CW) and ~41 nm min^{-1} (Pulse) for TiO_2 with BCl_3/Ar. (a) Normalized etch rates of Si and TiO_2 patterned with PR as a function of the aspect ratio (1.0~2.5 with the feature size of 150 nm). The normalized etch rates of Si patterned with electron beam resist (EBR) as a function of the aspect ratio (2.0~5.0 with the pitch size of 420 nm) are also shown. (b) Etch selectivities of Si/PR, Si/EBR, TiO_2/PR as a function of aspect ratio. Aspect ratio was estimated by the ratio of pattern depth/pattern open width.

aspect ratio of 1.0, the normalized etch rate for the CW bias condition was 0.81 and, as the ratio is increased to 2.5, the etch rate was decreased to 0.66. Therefore, the aspect ratio dependent etching (ARDE) effect was observed for both TiO_2 and Si. For the CW bias etching of Si patterned with E-beam resist (EBR) to the aspect ratio of 5.0, the effect of ARDE was more significant and, at the ratio of 5.0, the normalized etch rate was 0.5 (that is, compared to the etch rate of blanket Si, the etch rate of Si with the ratio of 5.0 was decreased to 50%). However, for the pulse biased etching, at the aspect ratio of 1.0, the normalized etch rate of TiO_2 was 0.99 and that of Si was 0.94, therefore, much less ARDE effect could be observed for the pulsing. Also, as the ratio is increased to 2.5 and 2.8 for PR patterned Si and TiO_2, respectively, the normalized etch rates by the pulsed bias etching were higher than those by CW bias etching by showing the normalized etch rates of 0.85 and 0.93 for Si and TiO_2 at the ratio of 2.5 and 2.8, respectively. For the Si with ratio of 5 by EBR, the normalized etch rate was also higher as 0.64 for the pulse bias etching compared to 0.5 for CW bias etching, therefore, much less ARDE effect was observed by the pulse bias etching. In addition to the line-patterned Si and TiO_2, the etch rates of pillar-pattern were also measured at the same conditions. In the case of pillar (nanopost) patterns, the decrease in the etch rates with decreasing the pitch size, that is, with increasing aspect ratio, the ARDE effect was also observed but the differences in etch rates were much smaller due to much larger open area compared to feature size for pillar pattern at the same aspect ratio.

Figure 3(b) shows the etch selectivities of Si/PR, TiO_2/PR, and Si/EBR measured as a function of the aspect ratio for the conditions in figure 3(a). As shown in figure 3(b), the etch selectivities for the CW bias etch condition were remaining similar at ~3.25 for Si and at 2.75~2.25 for TiO_2 regardless of the aspect ratio for the ratio of 1.0~2.8 with PR. The etch selectivitiy of Si/EBR was lower than that of Si/PR, but, the etch selectivities were also not significantly varied with the aspect ratio of 2.0~5.0 by showing 1.3~1.1. Pulse bias etching instead of CW bias etching did not improve the etch selectivity by showing a little lower etch selectivity for PR patterned Si and TiO_2, 2.9~3.1 (3.25 for CW) and 1.8~2.0 (2.75~2.25 for CW), respectively, while the etch selectivity of Si/EBR for the pulse bias condition was a little higher at 1.8~1.9 (1.3~1.1 for CW). But, the etch selectivity for the pulse bias condition was not also significantly varied with the aspect ratio similar to the CW bias condition.

Figure 4 shows the etch profiles of silicon (a,b) and TiO_2 (c,d) patterned with photoresist having different aspect ratios of line (nanograting) and pillar (nanopost) patterns. Si and TiO_2 were etched using CW biasing (a,c) and pulse biasing (b,d) while applying CW rf power to the ICP source. As shown in figures 4(a) and (b), the differences in the etch depth between the large pitch pattern (center) and small pitch pattern (left) were larger for the CW biasing compared to pulse biasing and, for silicon pillar pattern (right), smaller etched feature width at the bottom of the feature was observed for CW biasing compared to pulse biasing. Larger differences in the etch depths were also observed for TiO_2 etching for CW bias etching compared to pulsed bias etching as shown in figures 4(c) and (d). For CW bias etching, trenching was also observed during the etching. Figure 5 shows the etch profiles of silicon pillars patterned with EBR of different feature widths. EBR patterned silicon pillars were etched partially (a,c) and completely (b,d) by CW bias etching (a,b) and pulse bias etching (c,d). Silicon thickness was 300 nm and the pattern opening widths were varied from 120 nm to 320 nm, therefore, the pattern opening widths were smaller than those in figure 4. As shown in figures 5(a) and (c), more significant differences between the largest pattern opening (right) and the smallest pattern opening (left) were observed for CW bias etching compared to pulse bias etching. Also, as shown in

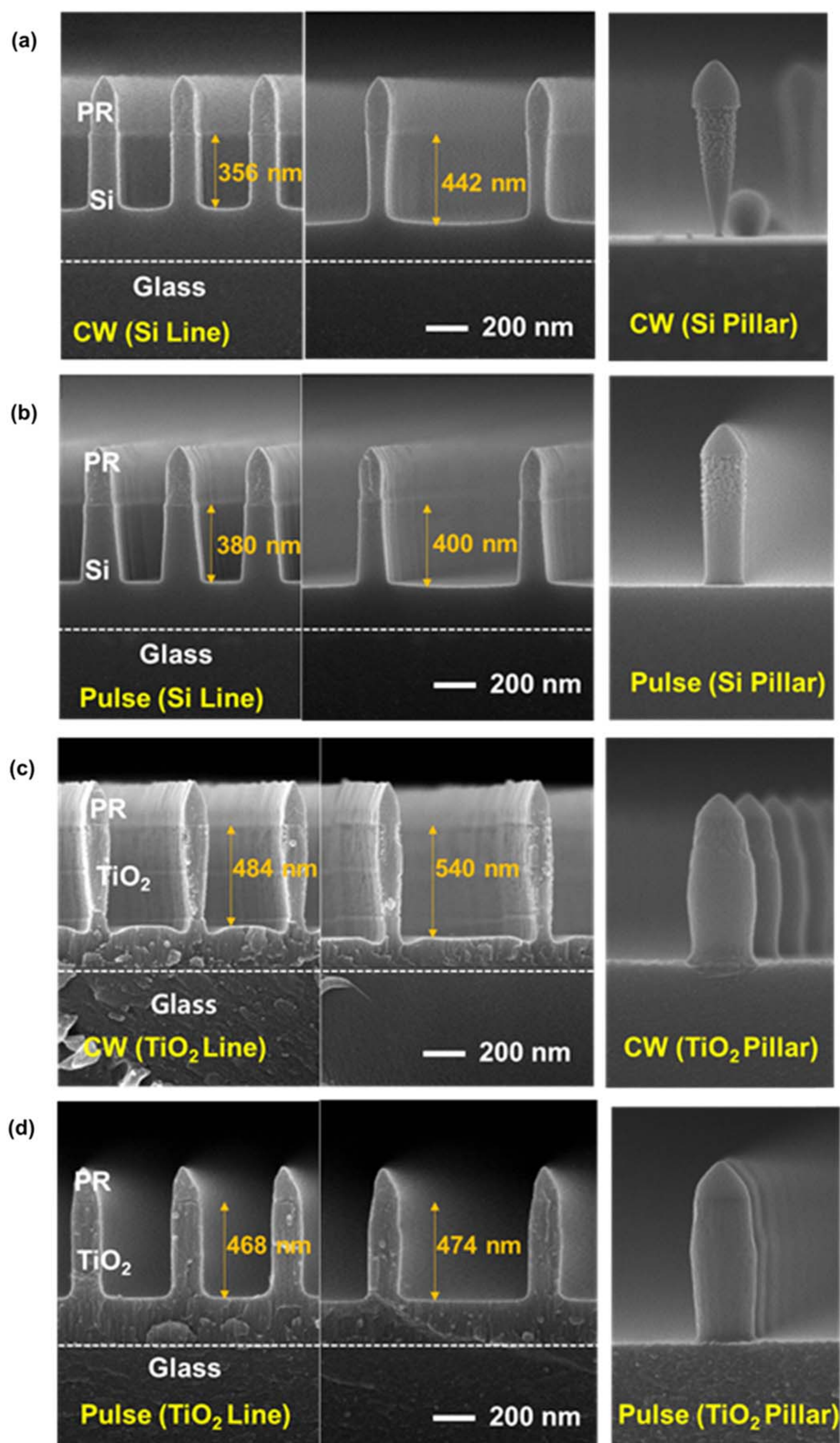

Figure 4. SEM images on etch profiles of silicon and TiO_2 patterned with photoresist having different aspect ratios of line (nanograting) and pillar (nanopost) patterns (a) CW bias etched Si, (b) Pulse bias etched Si, (c) CW bias etched TiO_2, (d) Pulse bias etched TiO_2.

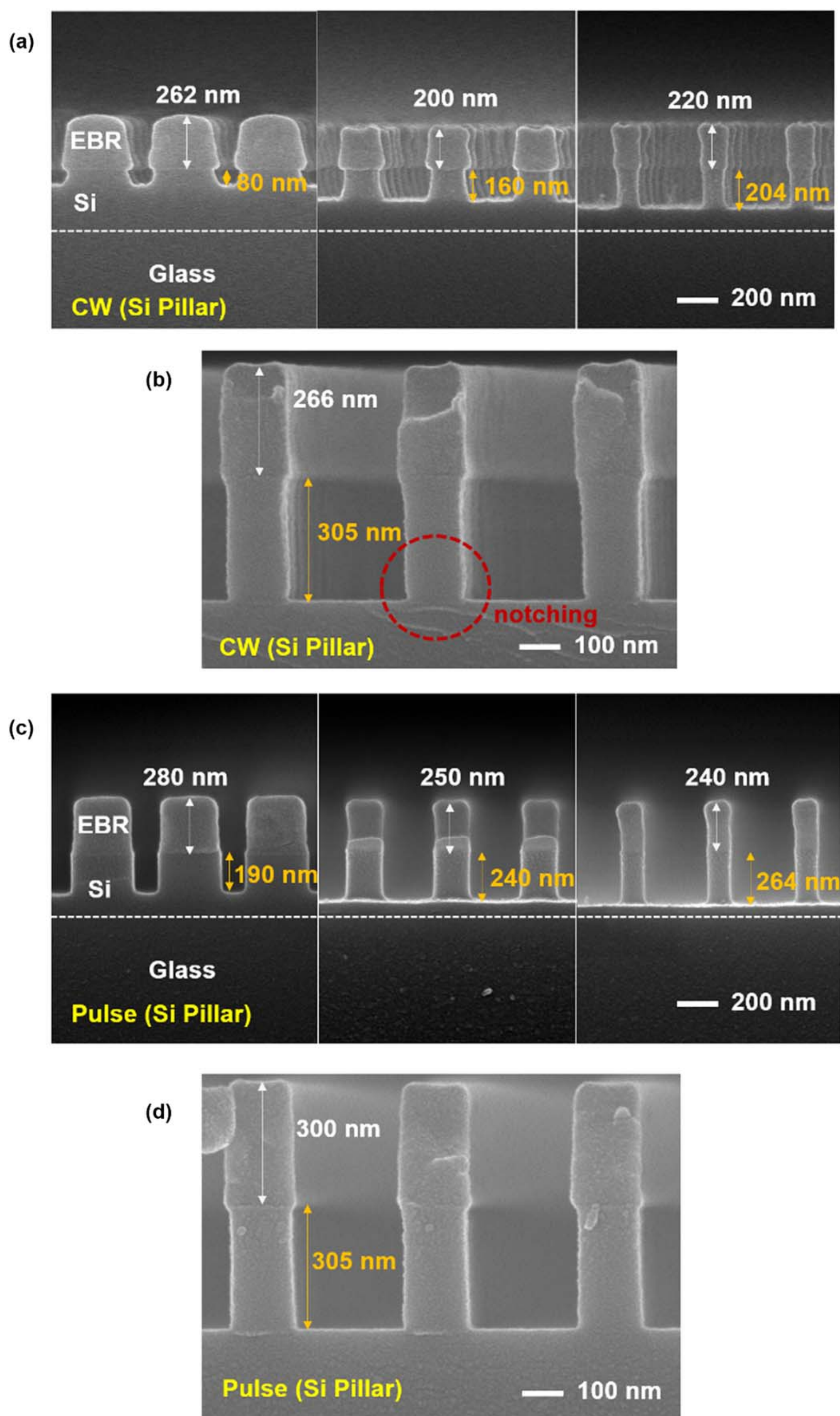

Figure 5. EBR patterned Si pillar etch profile with different feature width; (a) CW partial etch, (b) CW complete etch, (c) pulse bias partial etch, and (d) pulse bias complete etch.

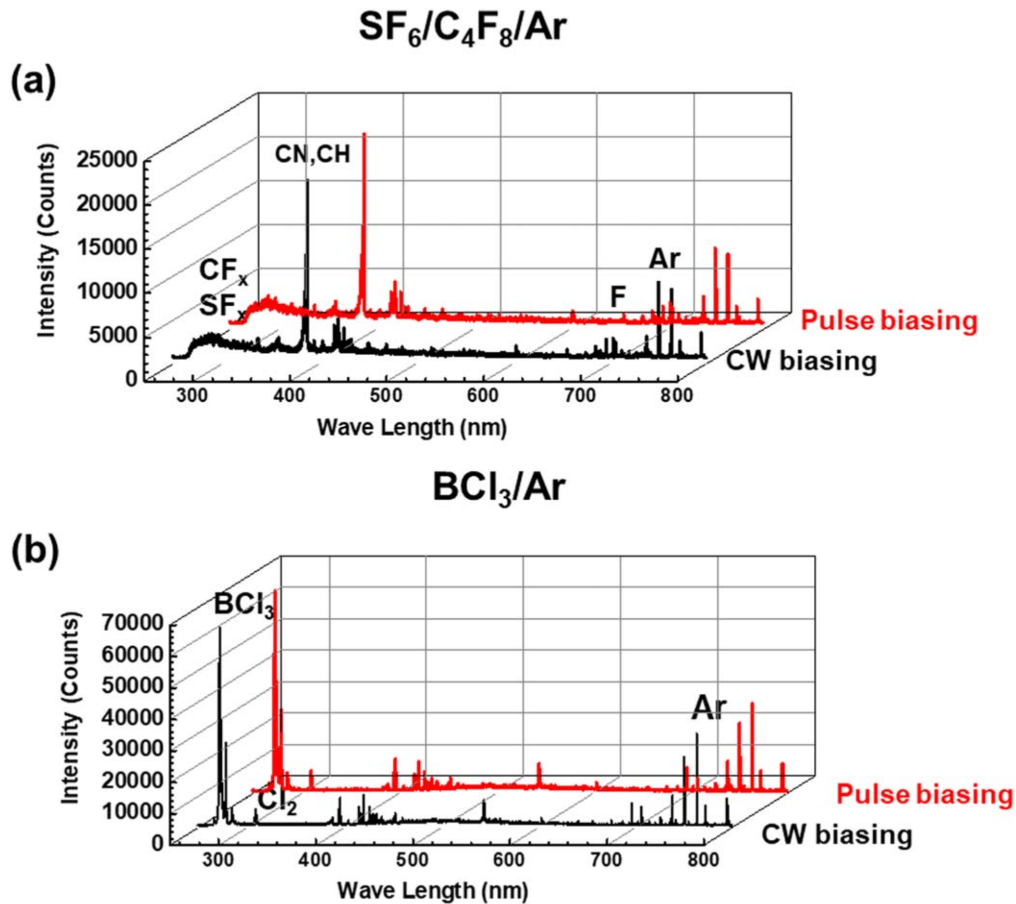

Figure 6. OES intensity during the operation of CW biasing and pulsed biasing with (a) $SF_6/C_4F_8/Ar$ plasma and (b) BCl_3/Ar plasma. For CW biasing and pulse biasing, −50 V of DC bias voltage was used to the substrate during the power-on with 13.56 MHz rf power and 700 W of CW 13.56 MHz rf power was used for the ICP source.

figures 5(b) and (d), after complete etching, a notching effect was observed for the silicon pillar etched by CW bias etching while no such notching was observed for the silicon pillar etched by pulse bias etching. Additionally, in figures 4(a) and (b), the sidewalls of the etched Si features for both pulse biasing and CW biasing conditions (right isolated features) show rough sidewall structures and, we believe those are related to the sidewall residue remaining during the etching. However, the source of the sidewall roughness is not clear and needs to be investigated further in the future works (in addition to the effects of other parameters that could affect the ARDE effect and etch profiles such as pulse duty ratios, gas flow, substrate temperature, etc).

The differences in the etch depths and etch profiles between the large pitch pattern (large pattern opening) and the small pitch pattern (small pattern opening), that is, ARDE effect, can be originated from various reasons. It can be originated from the differences in the conductance of etchants/etch products flowing in and out from the bottom surface of the feature (smaller pitch pattern has lower conductance than higher pitch pattern due to smaller gaps), from the differences in ion deflection to sidewall due to charging (smaller pitch pattern has lower ions arriving at the bottom surface of the feature due to more deflection of ions to the sidewall of the feature), etc. As shown in figures 3–5, with the use of pulse biasing instead of CW biasing, the ARDE effect was mitigated. To understand the reason for the decreased ARDE effect using the pulse biasing, characteristics of the plasmas and surface characteristics of the materials during the etching by CW biasing and pulse biasing were investigated.

Figure 6 shows the OES data of (a) $SF_6/C_4F_8/Ar$ plasma and (b) BCl_3/Ar plasma for CW biasing and pulse biasing used to etch silicon and TiO_2, respectively. As shown in figures 6(a) and (b), the use of pulse biasing instead of CW biasing did not change the OES peak intensities related to the dissociated species. It is believed that, the gas dissociation in the plasma is more related to the ICP source power than bias power conditions, therefore, the change of etch profiles by using pulse biasing instead of CW biasing appears not to be related to the change in radical species in the plasmas.

Figure 7 shows the ion energy distributions of (a,c) $SF_6/C_4F_8/Ar$ plasmas and (b,d) BCl_3/Ar plasmas measured at the substrate location using the RFA (ion energy analyzer) during the biasing the substrates by CW biasing and pulse biasing. Positive ions (a,b) and negative ions (c,d) were measured by applying different voltages to the three grids of the ion energy analyzer described in the experimental section. As shown in figures 7(a) and (b), during the biasing with the DC bias voltage of −50 V (during the power-on), the positive ions to the substrate surface with the energy distribution of

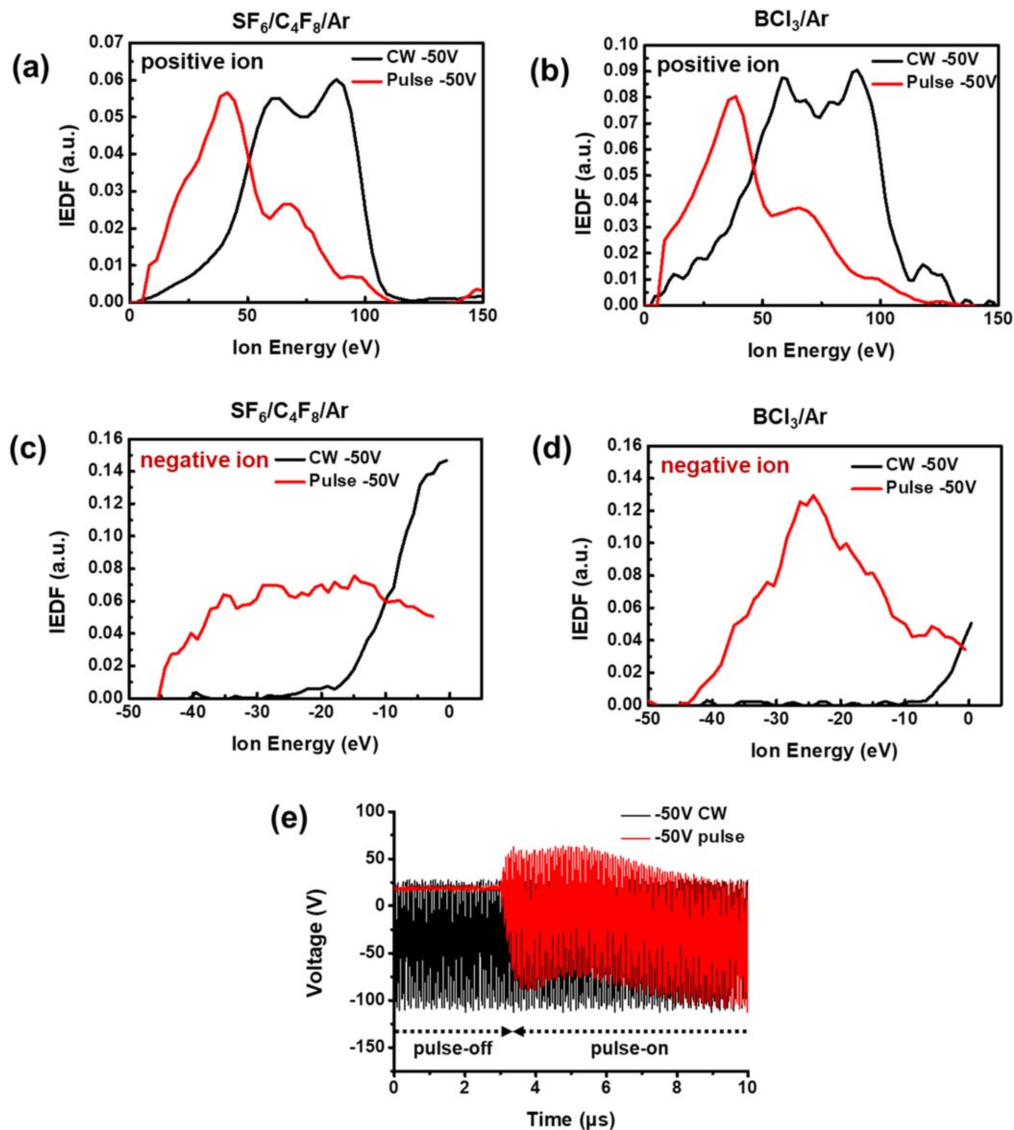

Figure 7. Positive ion energy distribution ((a) and (b)) and negative ion energy distribution ((c) and (d)) to the substrate during the operation of CW biasing and pulse biasing with $SF_6/C_4F_8/Ar$ plasma ((a) and (c)) and BCl_3/Ar plasma ((b) and (d)). (e) rf voltage shapes measured as a function of time for CW biasing (black color) and the initial pulse-on period of pulse biasing (red color) with 13.56 MHz rf power to the substrate with a $SF_6/C_4F_8/Ar$ plasma (−50 V of DC-bias voltage during power-on).

0∼120 eV could be measured using the ion energy analyzer (grid G1:−110 V, grid G2: varied −50∼100 V, grid G3: −120 V, C:−110 V) for both $SF_6/C_4F_8/Ar$ plasmas and BCl_3/Ar plasmas. Pulse biased plasmas showed less positive ion energies compared to the CW biased plasmas. As shown in figures 7(c) and (d), by using different grid voltages (G1:70 V. G2: varied −100∼0 V, G3: 60 V, C: 70 V) to the ion energy analyzer, negative ion (or electron) energy distribution could be measured. As shown in figures 7(c) and (d), the negative ion (or electron) energy distributions with 0∼45 eV were observed for pulse biased plasmas while much smaller energy distributions from 0∼(10) 20 eV were observed for CW biased plasmas. The differences in the energies of charged species to the substrate between the CW biasing and pulse biasing are believed to be related to the differences in rf voltage shapes during the operation with different substrate biasing. For CW biasing, the rf peak voltage is in the range of +10∼−110 V and stable. However, as shown in figure 7(e), for pulse biasing, no voltage is applied to the substrate during the half pulse-off cycle and, after pulse-on, rf peak voltage is decreased from +45∼−75 V to +10∼−110 V (similar to CW biasing). Therefore, higher negative ion (or electron) energies in addition to more negative ion species can be reached on the substrate surface by pulse biasing compared to CW biasing. The energetic negative ions (electrons) to the substrate by the pulse biasing can neutralize the sidewall surface of the etched surface and remove the charging effect which leads to profile distortion and ARDE effect.

Figure 8 shows the surface composition of (a) Si surface and (b) TiO_2 surface etched with the $SF_6/C_4F_8/Ar$ plasma and the BCl_3/Ar plasma, respectively, for CW biasing and pulse biasing by XPS. Two different regions of line pattern area (narrow open area) and pillar pattern area (wide open

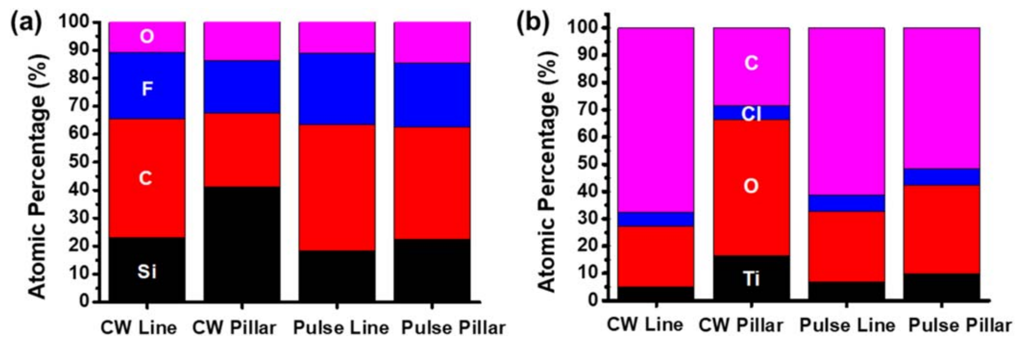

Figure 8. (a) Chemical composition of Si surface (narrow line area and wide pillar area) and (b) TiO_2 surface (narrow line area and wide pillar area) etched with CW biasing and pulse biasing measured by XPS.

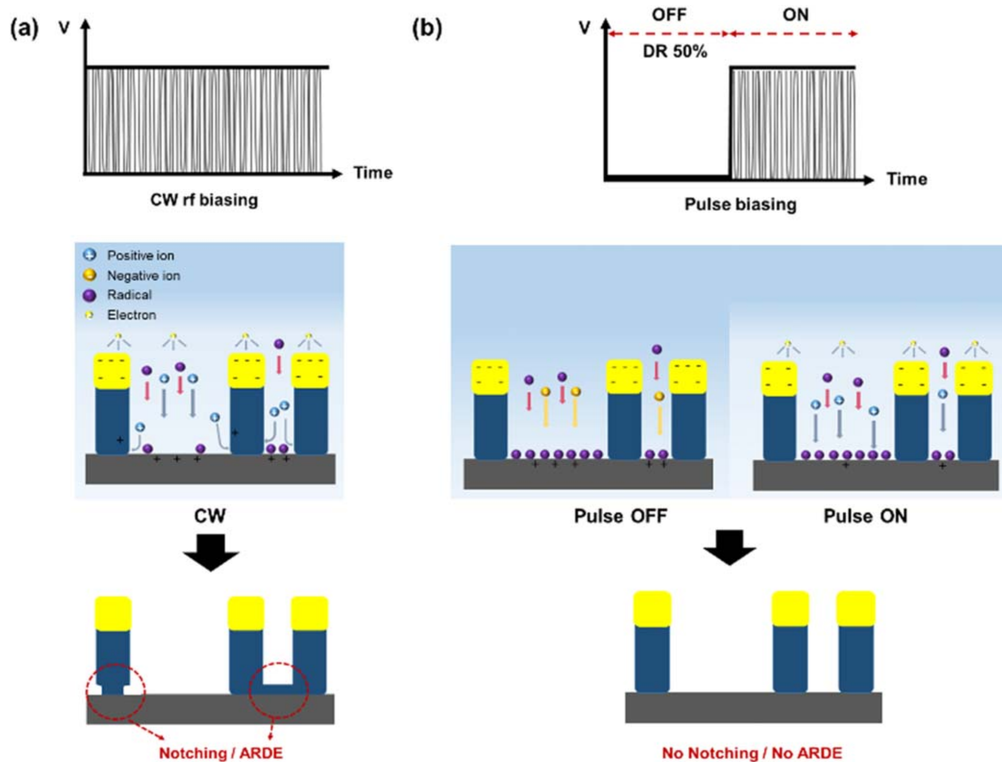

Figure 9. Diagrams of (a) surface charging by positive ions and decreased ions to the bottom surface for narrow gap area for CW biasing. (b) neutralization of surface charging by negative ions (electrons) and uniform radical arrival (etch product removal) during pulse-off period for pulse biasing.

area) were measured to study the effect of aspect ratio on the surface composition of the etched surfaces (due to the lack of large sample region with same line (or pillar) patterns with different aspect ratios which can be measured by XPS, instead, we used line pattern areas as the high aspect ratio area (narrow pattern open area) and pillar pattern areas as the low aspect ratio area (wide pattern open area)). As shown in figure 8(a), for pulse biasing, the surface compositions of Si, C, and F which includes a C_xF_y passivation layer are similar for both line pattern and pillar pattern while, for CW biasing, the surface compositions of Si, C, and F are different between the line pattern and pillar pattern. For TiO_2 etched surface, similar to the silicon etched surfaces, the surface compositions of line pattern and pillar patern were similar for pulse biasing while those were different for CW biasing. The similar surface composition on the etched surfaces of line pattern area and pillar pattern area for pulse biasing is believed to indicate the similar radical condition for all of the sample surfaces which leads to the similar etch rates for the features with different aspect ratios.

Figure 9 shows a possible mechanism for the improvement of etch profile and ARDE effect by using pulse biasing instead of CW biasing. As shown in figure 9(a), for CW biasing, due to the continuous high energy positive ions with low energy electrons, the bottom of the feature is charged positively while the top area is charged negatively. Due to the charging, a positive ion is deflected to the sidewall, notching appears at the corner of the etched feature (after full etching)

and the ARDE effect is observed. Surface chemical compositions are also different due to the differences in ion flux to the substrates between narrow pattern open area and wide pattern open area. However, for pulse biasing, as shown in figure 9(b), due to the removal of surface charging by energetic negative ions (electrons) and sufficient radical adsorption/etch product removal on the all etched surfaces during the pulse-off period, energetic positive ions arrive uniformly not only on the wide pattern open area but also on the narrow pattern open area during the pulse-on period without deflection to the sidewall, and which leads to the etching of features without notching and ARDE effect.

4. Conclusion

For the etching of silicon and TiO_2 nanograting (line)/nanopost (pillar) on glass substrates using a $SF_6/C_4F_8/Ar$ ICP plasma and a BCl_3/Ar ICP plasma, respectively, a pulse bias etching technique has been used and its effects on etch rates and etch profiles for the patterns with different aspect ratios were investigated and compared with CW bias etching. The pulse biasing showed lower etch rates compared to the CW biasing due to the pulse-off time, however, a reduced ARDE effect and better etch profiles without showing any notching were observed compared to CW biasing. The improvement of etch profiles and lower ARDE effect were related to the decreased surface charging and improved radical adsorption (or etch byproduct removal) on the etched feature surface during the pulse-off period during the pulse biasing. It is believed that the results of pulse biased plasma etching can be applied to the fabrication of various nanostructures including optical devices on glass substrates.

Acknowledgments

This study was supported by the Nano Material Technology Development Program through the National Research Foundation Korea (NRF), funded by the Ministry of Education, Science, and Technology (2016M3A7B4910429) and by the Samsung Electronics.

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